A 50MS/s (35mW) to 1kS/s (15µW) power scaleable 10b pipeline ADC with minimal bias current variation

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Using a novel opamp with a short power-on time, a 10b 1.5b/stage power scaleable pipelined ADC in 0.18µm 1.8V CMOS occupying 1.2mm^2 is presented. A Current Modulated Power Scaling (CMPS) technique is used to multiply the power scalable range of current scaling, such that power varies between 15µW (1kS/s) and 35mW (50MS/s) (i.e. 2500x), yet bias currents are only varied 50x. SNDR is 54-56dB for all sampling rates (f_s). This work was the first published ADC [1] with wide variations in power with f_s without commensurate variations in bias current.

A power scaleable ADC is motivated by applications which e.g.: are required to operate at different f_s, have multi standard compliancy, or have varying input bandwidths. A power scaleable ADC is also of great utility in industrial applications, as only a single ADC is required for design to target a broad array of applications with different performance requirements (e.g. from low power biomedical to high speed data communications). Noting that otherwise several different ADCs each power optimized for only a single f_s would have to be designed and tested.

Although digital power scales explicitly with operating speed according to $0.5f_sCV^2$, analog power (the dominant power consumer in ADCs) does not explicitly scale with sampling rate as it is static in nature. Previous publications scale power in ADCs by making opamp bias currents a function of sampling rate [2], [3]. Extended bias current variations to maximize the power scaleable range however force current mirrors into weak inversion. As current mirrors in weak inversion are known to suffer from large process variations, weak inversion operation results in an ADC which suffers from poorer yield and accuracy.

To attain power scalability in this work, it is noted that if bias currents are unaltered while f_s is decreased, the settling time (t_{settle}) of analog blocks in an ADC becomes a smaller percentage of the period. By latching the ADC's digital outputs after t_{settle}, the analog portion of the ADC can be completely powered off shortly thereafter as shown in Fig. 1. This results in an average ADC power of: $P_{avg}=P_{ON}t_{ON}f_s$ ($t_{ON}=t_{settle}+t_{latch}$; P_{ON} the power consumed during t_{ON}).Lower power for lower sampling rates is realized only by changing the time the ADC is powered off (t_{OFF}), and without adjusting bias currents. Thus strong inversion performance can be retained for low sampling rates. If however bias currents are also scaled in conjunction with CMPS, CMPS multiplies the power scaleable range of current scaling as shown in Fig. 2.The lowest power achievable with CMPS is limited by blocks that consume non-zero average power during t_{OFF}. The highest f_s attainable with CMPS is limited by how quickly the ADC can power-on after t_{OFF}.

CMPS was applied to a 10b 1.5b/stage pipeline as shown in Fig 3. A state machine controlled the power timing of each block in the ADC (Fig 4). CMPS limits the maximum f_s to 1/(total ADC latency)=5.55MS/s. To achieve power scalability up to the maximum speed attainable with a pipeline approach i.e. 1/(single stage latency)=50MS/s, the ADC was operated as a conventional ADC (i.e. CMPS disabled) between 5.55MS/s and 50MS/s, with current scaling used to achieve power scalability for these f_s. Current scaling by 1:9 multiplies the power scalable range of CMPS by 9. Since current scaling is required only over a minimum of a 1:9 variation in operating speed, weak inversion can be minimized and/or avoided through judicious design.

The key challenge in implementing CMPS at high speeds is to be able to rapidly power-on the opamps in the ADC. Using a feedback based approach, a rapid power-on opamp is proposed and shown in Fig. 6. Switching a copy of the bias voltage of an opamp's current source, rather than the bias voltage itself results in short power-on times, as the copied bias voltage has a much shorter slew time due to a much smaller capacitance and higher driving current. Since the feedback increases current source's output resistance, a large DC gain is also achieved by using the approach in a single-stage folded cascode gain-boosting architecture, affording simple load compensation and passive common-mode-feedback. Series current switching is used to power on/off the feedback-opamp and all tail current transistors during t_{OFF} without affecting the signal swing at the output of the opamp. MOS switches in Fig. 6 are used to decrease power-off time, and avoid floating nodes during t_{OFF}.

Fig 7 shows the measured power vs. sampling rate of the ADC, where CMPS is used between 1kS/s and 5.55MS/s, and current scaling between 1MS/s and 50MS/s. The different individual curves correspond to different clock rates of the state machine (f_{sm}). The lowest power for a given f_{sm} is limited by the state machine's power; hence f_{sm} is reduced between 50MHz and 1MHz to maximize the power scaleable range. The measured results show that CMPS multiplies the power scaleable range of current scaling by 50x, resulting in an overall power scaleable range of 1:2500. Fig. 5 shows the performance at the maximum speed of 50MS/s, where an SNDR of 55dB is achieved at f_{in}=20.94MHz, and SFDR of 67dB. The INL at f_s=50MS/s was +1.06/-1.2, and DNL +0.63/-0.91. Fig. 8 compares this work with recently published and commercial 10b ADCs.

References:

[1] I. Ahmed, D. Johns, "A 50MS/s (35mW) to 1kS/s (15µW) power scaleable 10b pipelined ADC with minimal bias current variation", *ISSCC Dig. Tech. Papers*, pp. 280-281, Feb 2005

[2] K. Gulati, H.S. Lee, "A Low-Power Reconfigurable Analog-to-Digital Converter", *IEEE J. Solid State Circuits*, vol 36, pp. 1900-1911, Dec. 2001

[3] B. Hernes et al, "A 1.2V 220MS/s 10b Pipeline ADC Implemented in 0.13µm Digital CMOS", *ISSCC Dig. Tech. Papers*, pp. 256-257, Feb. 2004

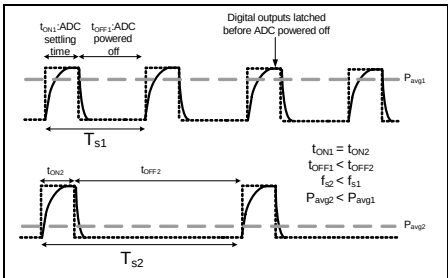

Fig. 1: CMPS with fixed bias

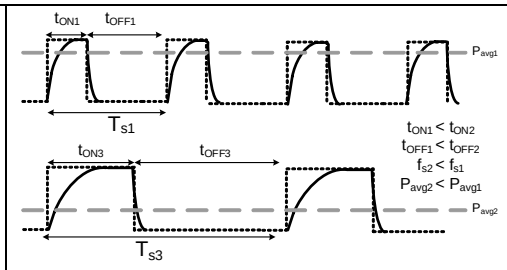

Fig. 2: CMPS with current scaling

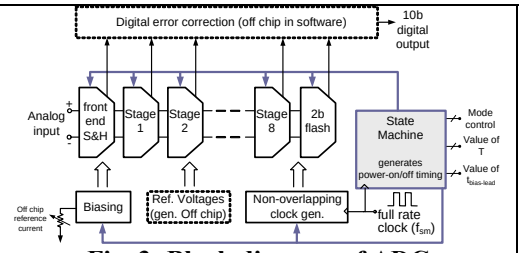

Fig. 3: Block diagram of ADC

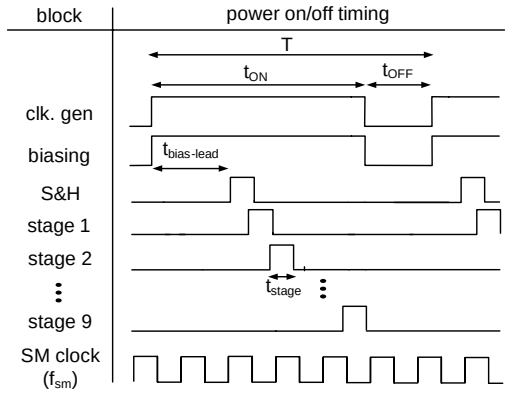

Fig. 4: Power on/off timing of each stage by state machine

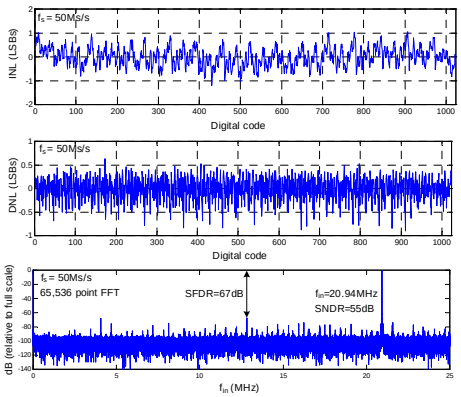

Fig. 5: Measured INL, DNL and output FFT at 50MS/s

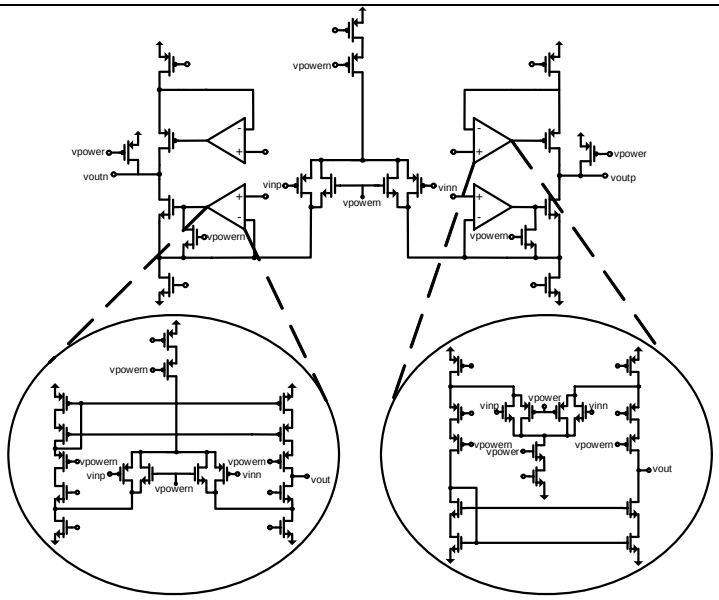

Fig. 6: Novel rapid power-on opamp

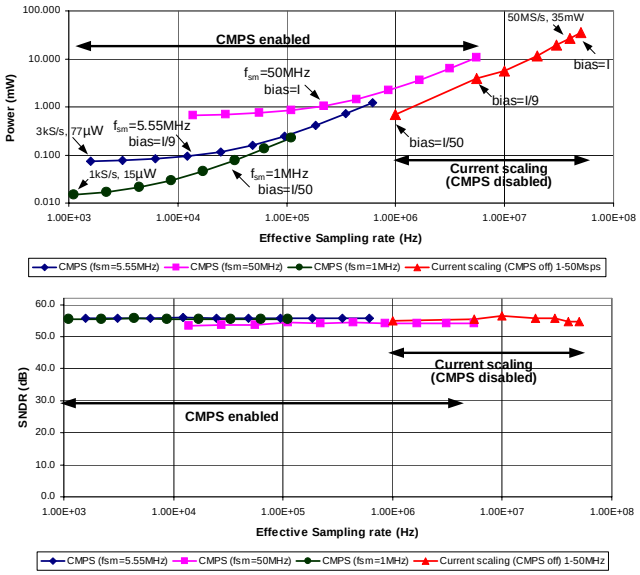

Fig. 7: measured power, SNDR vs. sampling rate

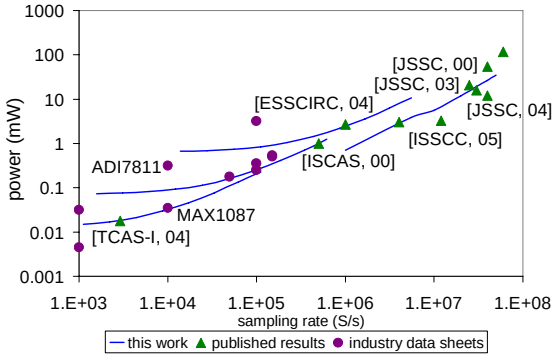

Fig. 8: Comparison of this work with other 10b ADCs

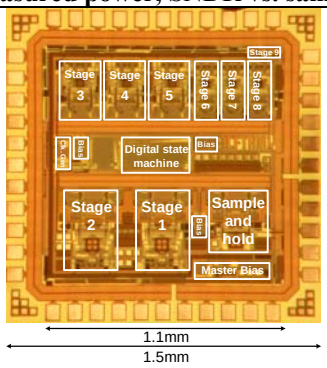

Fig. 9: Photograph of fabricated ADC