Monolithic DC-DC Boost Converter with Current-Mode Hysteretic Control

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***Abstract*—A monolithic DC-DC boost converter with current-mode hysteretic control is designed and simulated in 0.18-μm CMOS technology. The system is simple, robust, and has a fast response to external changes. It does not require an external clock, and the output is regulated by voltage feedback in addition to limiting the inductor current by sensing it. A non-overlapping clock is internally generated to drive the power switches using buffers designed to minimize power dissipation. For conversion specifications of 1.8 V to 3.3 V at 150 mA, overall efficiency of 94.5% is achieved. Line regulation is 17.5 mV/V, load regulation is 0.33% for a 100 mA current step, while the output voltage ripple is below 30 mV for nominal conditions.**

I. Introduction

The market for hand-held and portable electronic applications is a driving force behind significant technological advances. As device sizes continue to get smaller, reducing silicon area, the power dissipation of digital circuits is reduced by scaling down the supply voltage. At the same time certain circuits have specific voltage requirements that do not follow the same scaling pattern. As more and more functions are integrated on to a micro-system, the required voltages are internally generated from a single power supply. Increasingly, integrated Power Management Units (PMUs) are being used to cater to distinct and varying power needs of each part of the micro-system by employing DC-DC converters.

For portable applications that run on batteries, efficient operation of converters is essential over a wide range of currents. Even though such circuits must be designed to effectively deliver a nominal current, portable devices have various operating modes including low-power modes which require lower currents. Other parameters that determine the performance include line regulation (adjusting to varying input voltage) and load regulation (adjusting to varying load current). The output voltage ripple is of interest in some applications as well. This paper focuses on the design of a control system for the boost converter, which is critical to the converter's performance. A hysteretic control technique is applied to a boost converter and is evaluated with regards to line regulation, load regulation, transient response, and output voltage ripple.

II. Boost Converter Design Issues

The choice of a control system determines the frequency, duty cycle, and transient behavior of a converter among other things. Typically either Pulse Width Modulation (PWM) or Pulse Frequency Modulation (PFM) are used to regulate the output voltage in boost converters [1]. PWM is a widely used scheme that provides accurate regulation at a constant frequency. The fixed frequency of PWM control enables the output voltage ripple to conform to a known frequency spectrum profile, thus enabling simple filters to reduce voltage ripple (and control by the designer to avoid exciting resonant modes in the system). However, its response, to sudden changes in output is relatively slow, it has lower efficiency at light loads, and may require large on-chip components required for compensation to ensure loop stability. On the other hand PFM control can provide higher efficiency at light loads because of low quiescent currents.

A current-mode hysteretic control for a boost converter is investigated for this work. If the load current or input voltage of the converter change, the frequency is adjusted by the controller to compensate for the change. Hysteretic control has a fast transient response [2], and is inherently stable over a much wider range of values of L and C than PWM. While abundant literature is available for hysteretic buck converters, such material is lacking with regard to integrated boost converters. This is probably due to the fact that hysteretic control is not readily applicable to boost converters [3], in which the presence of a right-half-plane zero complicates the design. In buck converters, voltage-mode control may be used to set a hysteresis window by comparing the output voltage alone. However, this cannot be done in boost converters because the output voltage and the inductor current are out of phase with each other. The compensation of hysteretic boost converter can be done using an RC network and an auxiliary winding of the inductor [4]. This introduces additional off-chip components which will incur cost. An alternate technique [2] employs an auxiliary switch across the inductor and a charge pump in the feedback loop for a hysteretic system, a solution that requires access to both terminals of the inductor.

To minimize the number of pins and interconnects (thus chip and board area), our work is constrained to only two points of access: an input through the inductor and the output voltage for feedback. Therefore a solution other that proposed in [2] must be found. A hysteretic control system is implemented by employing the feedback voltage in addition to the sensed inductor current. The resulting circuit is simple and robust with fast transient response.

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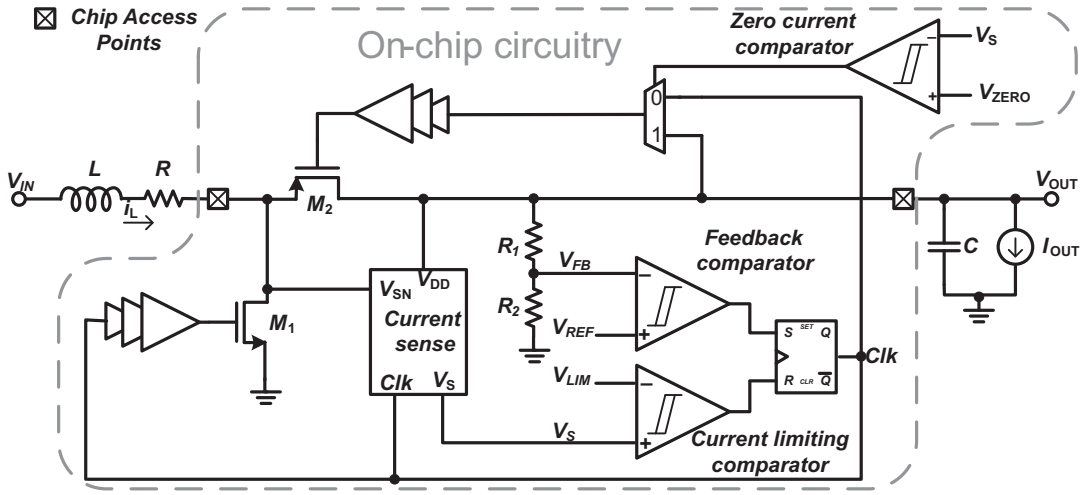

Fig. 1. System block diagram of the converter.

III. System Architecture

The system architecture is shown in Fig. 1. In steady state, the current sense block generates a voltage V_S proportional to the current flowing through the inductor. The current sensor is designed so that a current on the order of hundreds of milliamperes is replicated as a corresponding voltage V_S of hundreds of millivolts. This voltage is used to limit the maximum current that can flow through the inductor using a current limiting comparator with a reference voltage V_{LIM}. The outputs of the feedback and current limiting comparators are used to generate a clock by an SR latch that switches the two power transistors. The switching action is initiated when the threshold set by V_{LIM} (the upper limit of the output voltage) is reached by V_S. At this point, the current limiting comparator output resets the SR latch which sets the clock signal low, thus turning off power transistor M_1 and turning on power transistor M_2. The lower limit of the output is set by V_{REF}, which is derived from a bandgap reference voltage. V_{REF} is compared with the feedback voltage, which is scaled down using the voltage divider formed by R_1 and R_2, the ratio of which determines V_{OUT}. The output of the feedback comparator sets the SR latch, which makes the clock signal high and switches the power transistors.

An additional benefit of this architecture is that it does not require extra circuitry for over-current protection, since the current limiting comparator does not allow the current to go above the value determined by V_{LIM}.

The significant functions of the overall circuit are briefly explained in the following sections.

A. Current Sensing

Current sensing circuits for DC-DC converters mostly involve sensing the current for the phase of the switching cycle that charges the inductor [5], while the sensed voltage for the discharging phase is zero. This is sufficient for buck converters and boost converters with a diode instead of the pMOS switch. For the topology shown in Fig. 1, the peak current for the whole switching cycle needs to be sensed for the current limiting aspect of the architecture, while information on the minimum current is required to prevent the inductor current from reversing direction. The inductor current is sensed by a circuit similar to one proposed in [6], where the current for the entire clock cycle is replicated.

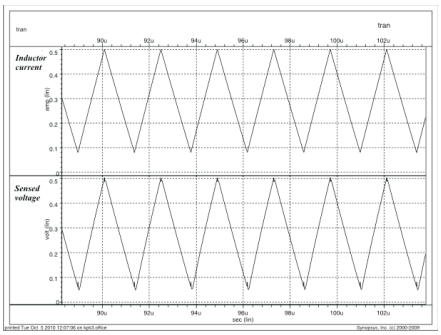

Fig. 2. Transient simulation of inductor current (top) and sensed voltage.

Fig. 2 shows a simulation of the inductor current and the sensed voltage produced by the current sensor on the same scale. The current does not need to be replicated exactly to have accurate regulation because in addition to the current sense loop, the feedback voltage loop is also involved in voltage regulation. If there is a large discrepancy, however, the ripple of V_{OUT} will be affected because of the change in the peak inductor current. This adds to the robustness of the system because device mismatches and process variations can introduce a discrepancy between the current and the corresponding voltage. The effect of a mismatch is observed with change in the peak-to-peak inductor current, and can be compensated for by adjusting V_{LIM}. V_{LIM} is selected (0.5 V in this case) such that under typical conditions, the minimum inductor current comes close to zero without sending the converter into DCM.

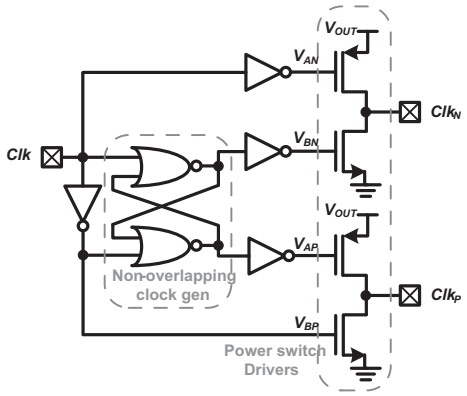

Fig. 3. Simplified diagram of power switch drivers.

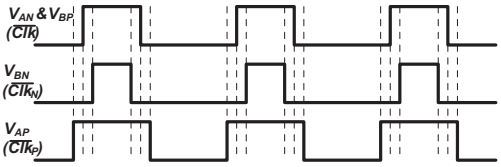

Fig. 4. Non-overlapping clocks.

TABLE I
NOMINAL COMPONENT VALUES AND REFERENCE VOLTAGES

L	4.7 μH	V_{REF}	1.25 V
C	20 μF	V_{LIM}	0.5 V
L_{ESR}	25 $m\Omega$	R_1	1 $k\Omega$
C_{ESR}	50 $m\Omega$	R_2	1.64 $k\Omega$

B. Zero-Current Detection

If the load current falls below a certain value (determined by the passive components), the converter enters DCM. This causes the inductor current to be negative for part of the switching cycle, causing the efficiency to suffer. In order to avoid negative inductor current, the pMOS switch M_2 needs to be turned off as the inductor current approaches zero. As shown in Fig. 1, this is done through a zero current comparator by comparing the sensed voltage V_S with a very small voltage (20 mV). This value is not particularly critical and can be chosen to be as low as 10 mV and as high as 50 mV, as long as it is above zero because during DCM the sensed voltage across the resistor approaches zero but does not become negative. The output of the zero current comparator controls a multiplexer, which alters the clock driving M_2 accordingly.

C. Power Switch Drivers

M_1 and M_2 in Fig. 1 are driven through the same clock signal, so there exists a possibility of short-circuit currents through the converter in case both switches are on during transitions. To avoid this condition, a non-overlapping (NO) clock generator is added to the path between the RS latch and the drivers. In addition, since the drivers are powered from the output voltage, it is necessary to introduce a NO scheme to drive them to avoid short-circuit (crowbar) currents that could introduce transient glitches in the output. Driver design is shown in Fig. 3, where the inverters nMOS and pMOS transistors can be half the size of those used in a conventional design. The circuit in Fig. 3 generates three NO phases which avoid short-circuit currents both in the power switches and in their drivers while keeping the NO time to the minimum. This improves the overall efficiency of the converter. Clocks for the drivers are sketched in Fig. 4.

IV. SIMULATION RESULTS

The boost converter was designed and simulated in 0.18-μm CMOS technology using 3.3 V high-voltage transistors. Component values and reference voltages for operation under nominal conditions (V_{IN} = 1.8 V, V_{OUT} = 3.3 V, I_{LOAD} = 150 mA) are given in Table I. Simulations were performed to test the circuit's robustness in regards to efficiency, line regulation, load regulation, and output voltage ripple over a range of load currents and input voltages.

Depending on component values, input voltage, and output current, the circuit adjusts the switching frequency which was observed to be 334 kHz for nominal conditions. Fig. 5 shows how the frequency is adjusted to compensate for change in load current. The increase in frequency as load current increases is almost linear up to a point, after which there is a rapid incline. This point is determined by the current limiting voltage V_{LIM}, which controls the peak inductor current. To reduce the frequency at higher currents, V_{LIM} can be raised, and vice-versa.

Simulations were also done to account for process variation and mismatches. Nominal (40°C), slow (both pMOS and nMOS, 120°C), and fast (both pMOS and nMOS, -40°C) corners were simulations were done and no appreciable impact on overall efficiency was observed. Owing to the fact that R_1 and R_2 are on-chip resistors, a slight variation in V_{OUT} occurs. For the fast-fast case, V_{OUT} rises by 20 mV, while it is reduced by 33 mV for the slow-slow case.

A. Efficiency

The system was designed to for maximum efficiency at the nominal specifications of V_{IN} = 1.8 V, V_{OUT} = 3.3 V, and I_{LOAD} = 150 mA. Efficiency versus load current for a number of input voltages versus load current is plotted in Fig. 6. The peak efficiency occurs at the initial specification value

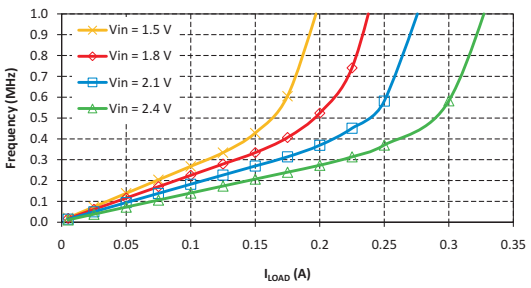

Fig. 5. Switching frequency vs. load current.

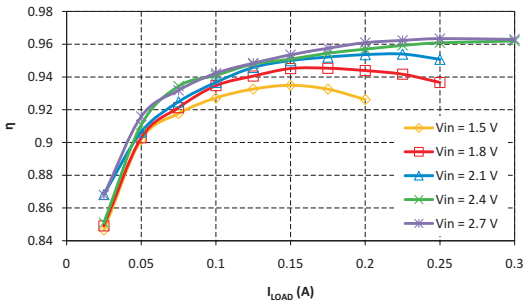

Fig. 6. Efficiency vs. load current for various input voltages.

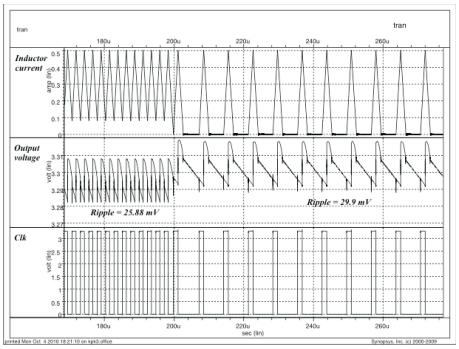

Fig. 7. Transient simulation of load change from 200 mA to 100 mA at V_{OUT} = 3.3 V.

of I_{LOAD} = 150 mA for V_{IN} = 1.8 V, and the efficiency remains above 90% for a wide range of current values starting at approximately 50 mA. Although the circuit works for input voltages of up to 3.3 V, voltages up to 2.7 V are shown to maintain clarity in the plots.

B. Load Regulation

V_{OUT} is regulated by adjusting the switching frequency. Fig. 7 shows a transient simulation where the load current (top waveform) is changed at 200 μs from 200 mA to 100 mA. It takes only a couple of cycles for the inductor current to settle into its new steady-state. At I_{LOAD} = 100 mA, the converter enters discontinuous mode, as is evidenced by inductor current flattening at zero. The middle waveform shows V_{OUT}, which rises by about 11 mV at 200 μs and does not exhibit overshoot or undershoot. The bottom waveform shows the how the frequency of the clock driving the nMOS power switch changes with the load current.

C. Line Regulation

The circuit is well suited for line regulation because of the availability of inductor current information in one of the control loops. Fig. 8 shows a transient simulation where the input voltage is varied from 1.5 V to 2.4 V. As with the load regulation plot, the current waveform, output voltage, and nMOS clock are shown.

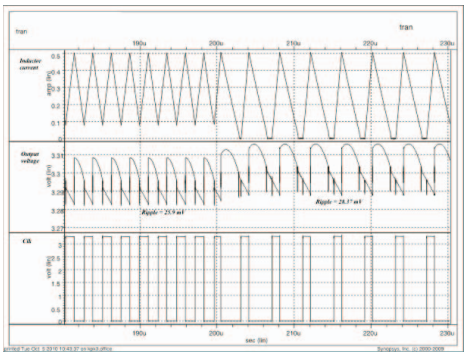

Fig. 8. Transient simulation of voltage change from 1.5 V to 2.4 at 150 mA at I_{LOAD} = 150 mA.

TABLE II
NOMINAL COMPONENT VALUES AND VOLTAGE RIPPLE

L	C	Voltage Ripple (mV)
2.35 μH	10 μF	26.3
	20 μF	26.2
	40 μF	26.3
4.7 μH	10 μF	32.7
	20 μF	25.9
	40 μF	26.3
7.05 μH	10 μF	43.3
	20 μF	28.4
	40 μF	25.7

D. Output Voltage Ripple

For V_{IN} = 1.8 V, V_{OUT} = 3.3 V, and I_{LOAD} = 150 mA, output voltage ripple is below 30 mV. If load current is reduced to 5 mA, ripple increases to about 38 mV. If V_{IN} = 2.7 V, V_{OUT} = 3.3 V, and I_{LOAD} = 150 mA, the ripple becomes almost 40 mV. Its values at nominal conditions if L and C are varied by $\pm$50% is listed in Table II.

V. CONCLUSION

Results of a current-mode hysteretic boost converter designed in 0.18-μm CMOS technology are presented. The system has a simple architecture and simulation results demonstrate a robust circuit with fast transient response. An efficiency of over 90% is achieved for a wide load current range. Good line and load regulation are demonstrated with fast transient response times.

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