Volume 10
Number 3
September
2005

SOLID-STATE CIRCUITS

IEEE Solid-State Circuits Society Quarterly Newsletter

Jaeger Elected President of SSCS; Willy Sansen Elected Vice-President

At their August 29 meeting, the Society Administrative Committee elected Dick Jaeger to serve as President of the Society beginning 1 January 2006. Willy Sansen was elected to serve along with Jaeger as Vice-President. It is typical after serving two years, the Vice-President is elected President by the AdCom.

Sansen will be the first non-US based officer of the Society, the membership of which is made up of equal numbers of US and non-US based members. The President and Vice-President must have served in elected or appointed AdCom positions.

Richard C. Jaeger has served as an elected AdCom member since 1999. He has been Publications chair since the inception of the Society, and Vice President for the last two years.

He received BS and ME degrees in electrical engineering in 1966 and his Ph.D. degree in 1969, all from the University of Florida, Gainesville. From 1969 to 1979 he was with the IBM Corporation, working on precision analog design, I2L, microprocessor architecture, and low-temperature MOS device and circuit behavior. Since 1979 he has been at Auburn University, where he is Distinguished University Professor in Electrical and Computer Engineering. In 1984 he helped found the Alabama Microelectronics Science and Technology Center and served as director of the center until 2000. He currently serves as the interim director of the Auburn University undergraduate program in wireless technology, which he founded.

He has authored or co-authored over 200 technical papers and articles and three books: Introduction to Microelectronic Fabrication, Microelectronic Circuit Design, and Computerized Circuit Analysis Using SPICE Programs. From 1980 to 1982 he served as founding Editor-in-Chief of IEEE MICRO. He was elected Fellow of the IEEE in 1986. Dr. Jaeger was a member of the IEEE Solid-State Circuits Council from 1984 to 1991, serving the last two years as Council President. He was Program Chair for the 1993 ISSCC, Chair of the 1990 VLSI Circuits Symposium, Editor of the IEEE Journal of Solid-State Circuits from 1995-1998 and recipient of the 2004 IEEE Undergraduate Teaching Award.

Richard C. Jaeger
SSCS President
2006-2007

Willy Sansen
SSCS Vice President
2006-2007

Willy Sansen has served as an elected member of the SSCS AdCom from 1999 to 2001. He received the MSc degree in Electrical Engineering from the K.U.Leuven in 1967 and a Ph.D. in Electronics from the University of California, Berkeley in 1972.

In 1972 he was appointed by the National Fund of Scientific Research (Belgium) at the ESAT laboratory of the K.U. Leuven, where he has been a full professor since 1980. During the period 1984-1990 he was the head of the Electrical Engineering Department. Since 1984 he has headed the ESAT-MICAS laboratory on analog design, which counts about sixty members and which is mainly active in research projects with industry. He is a Fellow of the IEEE and is a member of several corporate boards of directors.

He was a visiting professor at Stanford University in 1978, in 1981 at the EPFL Lausanne, in 1985 at the University of Pennsylvania, Philadelphia, in 1994 at the Ulm Hochschule

Continued on page 2

this IN issue

Jaeger Elected President of SSCS: Willy Sansen Elected Vice-President . . 1
Society to Elect New AdCom Members . . 2
New Conference Showcases the Young and Hot Digital Consumer Age in Asia 4
Book Review: Delta-Sigma Data Converters 5
Most Downloaded CICC Article Features the Conference's Real-World Design Focus 6
DAC/ISSCC Student Design Contest Promotes Excellence 8
Call for Fellow Nominations 9
How to Become a Senior Member 9
Chapter Activities Feature Guest Speakers from Industry, Government and Academia 11
SSCS Events Calendar 12

Continued from page 1

fur Technik and in 2004 at Infineon, Villach.

Prof.Sansen is a member of several editorial and program committees of journals and conferences. He is cofounder and organizer of the workshops on Advances in Analog Circuit Design (AACD) in Europe. He is a member of the executive and program committees of the IEEE ISSCC, and was program chair of the 2002 ISSCC.

He has been involved in design automation and in analog integrated circuit design for telecommunications, consumer electronics, medical applications and sensors. He has supervised over fifty PhD theses in these fields. He has authored or coauthored twelve books and more than 550 papers in international journals and conference proceedings.

Society to Elect New AdCom Members

Eight candidates will vie for five positions on the SSCS Administrative Committee (AdCom) that governs the Society. Ballots will be mailed to members of the Society in the fall. Student members are ineligible to vote in this election.

The AdCom has responsibility for the overseeing of current and potential technical activities within the Society's field of interest. Elected AdCom members can expect to attend at least two yearly meetings. In addition, much of the Committee work is carried on by email, telephone, and fax throughout the year. The Solid-State Circuits Society currently sponsors The Journal of Solid-State Circuits, the International Solid-State Circuits Conference, the Custom Integrated Circuits Conference, the VLSI Circuits Symposium, and the new Asia Solid-State Circuits Conference. In addition, the Society cosponsors or technically cosponsors a number of other conferences and meetings.

The term of office is three years, beginning 1 January 2006. The five nominees receiving the highest number of votes from the Society membership will be elected. This year two of the candidates have already served one three-year term.

Wanda Gass

Wanda Gass received her BSEE degree in 1978 from Rice University and her MS in Biomedical Engineering from Duke-University in 1980. She has been with Texas Instruments since 1980, where she is a TI Fellow. She was a key contributor in the development of the first programmable DSP at TI for which she holds several strategic patents. During her career she has done work in VLSI design, algorithms for speech codecs, multiprocessor system design for speech recognition and image processing, silicon compilers for DSP functions, video compression VLSI architectures, and W-CDMA hardware and software implementations. Currently she defines the instruction set architecture for high-performance DSP processors. Ms. Gass is a Senior Member of IEEE. She is an active member in the the Solid-State Circuits Society and the Signal Processing Society. In the SPS she has served as Member (1990-1996) and Chair (1997-1999) of the Design and Implementation of Signal Processing Systems Technical Committee. She was General Chair of the Signal Processing System Workshops in 2004. In the SSCS she has served as Member (1995-1999) and Subcommittee Chair (2000-2005), ISSCC International Program Committee. She has served as Member, SSCS Ad Com (2003-2005).

IEEE Solid-State Circuits Society AdCom

President:
Stephen H. Lewis
University of California
Davis, CA
lewis@ecc.uc.davis.edu
Fax: +1 914 945 4160

Vice President:
Richard C. Jaeger
Alabama Microelectronics Center
Auburn University, AL

Secretary:
David A. Johns
University of Toronto
Toronto, Ontario, Canada

Treasurer:
Rakesh Kumar
Technology Connexions
Poway, CA

Past President:
Charles G. Sodini
Massachusetts Institute of Technology
Cambridge, MA

Other Representatives:
Representative to Sensors Council
Darin Young
Representative from CAS to SSCS
Domine Leenaerts
Representative to CAS from SSCS
Ian Galton

Newsletter Editor:
Lewis Terman
IBM T. J. Watson Research Center
terman@us.ibm.com
Fax: +1 914 945-4160

Elected AdCom Members at Large
Terms to 31 Dec. 05:
Anantha Chandrakasan
John Corcoran
Wanda Gass
Teresa Meng
Jan Sevenhans

Terms to 31 Dec. 06:
Brian Ackland
Gary Baldwin
Tom Lee
Jan Rabaey
Jan Van der Spiegel

Terms to 31 Dec. 07:
Bill Bidermann
David Johns
Terri Fiez
Takayasu Sakurai
Mehmet Soyuer

Chairs of Standing Committees:

Awards	David Hodges
Chapters	Jan Van der Speigel
Education	CK Ken Yang
Meetings	Anantha Chandrakasan
Membership	Teresa Meng
Nominations	Charles G. Sodini
Publications	Bernhard Boser

For detailed contact information,
see the Society Web page: *www.sscs.org*

For questions regarding Society business, contact the SSCS Executive Office.

Contributions for the November 2005 issue of the e-News **must be received by 16 October 2005** at the SSCS Executive Office.

Anne O'Neill, Executive Director
IEEE SSCS
445 Hoes Lane
Piscataway, NJ 08854

Tel: +1 732 981 3400
Fax: +1 732 981 3401
Email: a.oneill@ieee.org

Peter Gillingham

Peter Gillingham joined MOSAID in 1989 as Project Manager leading the design of DRAM and Synchronous DRAM products in densities from 1Mbit to 16Mbit. After taking a sabbatical he became Marketing Director, focusing on embedded memory for both graphics and networking applications, as well as advanced memory architectures such as SLDRAM. He was appointed to Vice President of MOSAID in June 1998. In this position he led MOSAID's successful patent licensing program. He was named Vice President and General Manager of the Intellectual Property Division in April 2001. He is currently focused on MOSAID's Semiconductor Intellectual Property business, developing and marketing reusable functional blocks for System-On-Chip applications.

Prior to joining MOSAID, Peter was a Senior IC Design Engineer at Mitel Corporation, developing analog and ISDN products. He earned a B.Eng. in Electrical Engineering in 1980 and an M.Eng. in Electronics in 1983, both from Carleton University. From 1980-81 he was engaged in postgraduate research in the area of switched capacitor circuits at l'Ecole Polytechnique Federale in Lausanne, Switzerland. From 1992-93 he attended Stanford University Graduate School of Business as a Sloan Fellow, earning an M.Sc. in Management.

Peter served on the ISSCC Technical Program Committee Memory Subcommittee from 1995-98, and the Technical Program Committee for the VLSI Circuits Symposium from 1998-2002. He was Guest Editor for Special Issues of the Journal of Solid State Circuits in November 1995 and November 1996. He has been an Associate Editor of the Journal of Solid State Circuits since 1996. He has 18 publications in reviewed journals and conferences and over 50 issued patents.

Ali Hajimiri

Ali Hajimiri received his Ph.D. in electrical engineering from the Stanford University. He was a Design Engineer with Philips Semiconductors, where he worked on a BiCMOS chipset for GSM and cellular units. He has also been with Sun Microsystems and Lucent Technologies. In 1998, he joined the Faculty of the California Institute of Technology (CalTech), Pasadena, where he is a tenured Associate Professor of Electrical Engineering and the director of Microelectronics Laboratory. Dr. Hajimiri is the author of the book The Design of Low Noise Oscillators and holds several U.S. and European patents.

He is an Associate Editor of the JSSC and a member of the Program Committee of the ISSCC. He has also served as an Associate Editor of TCAS-II, a member of the Technical Program Committees of the ICCAD, Guest Editor of the Transactions on Microwave Theory and Techniques, and on the Guest Editorial Board of Transactions of IEICE, Japan.

Dr. Hajimiri was selected to the top 100 innovators (TR100) list in 2004 and is a Fellow of Okawa Foundation. He is a recipient of the Teaching and Mentoring award at Cal Tech. He was a co-recipient of the ISSCC 1998 Jack Kilby Outstanding Paper Award, two times co-recipient of CICC's best paper awards, a three times winner of the IBM faculty partnership award, as well as a recipient of a National Science Foundation CAREER award. He is a cofounder of Axiom Microdevices Inc.

Paul Hurst

Paul J. Hurst (S'76-M'83-SM'94-F'01) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of California at Berkeley in 1977, 1979, and 1983, respectively. From 1983 to 1984, he was with UC Berkeley as a lecturer, teaching integrated-circuit design courses and working on an MOS delta-sigma modulator. In 1984, he joined the telecommunications design group of Silicon Systems Inc., where he was involved in the design mixed-signal CMOS integrated circuits for voice-band modems. Since 1986, he has been on the faculty of the Department of Electrical and Computer Engineering at the University of California at Davis, where he is now a Professor.

His research interests are in the area of analog and mixed-signal integrated-circuit design for signal processing and communication applications. Research projects have included work on data converters, filters, image process, and adaptive equalizers and timing recovery circuits for data communications. He is also active as a consultant to industry. Paul Hurst has served on the program committees for the International Solid-State Circuits Conference and the Symposium on VLSI Circuits. He was guest editor for the December 1999 issue of the Journal of Solid-State Circuits. He has served as associate editor for the Journal of Solid-State Circuits since 2001. He is a co-author of a college text book on analog integrated-circuit design. He was elected IEEE Fellow in 2001.

Akira Matsuzawa

Akira Matsuzawa received B.S., M.S., and Ph. D. degrees in electronics engineering from Tohoku University, Sendai, Japan, in 1976, 1978, and 1997 respectively. In 1978, he joined Matsushita Electric Industrial Co., Ltd. Since then, he has been working on research and development of analog and mixed signal LSI technologies; ultra-high speed ADCs, intelligent CMOS sensors, RF CMOS circuits, digital read-channel technologies for DVD systems, ultra-high speed interface technologies for metal and optical fibers, a boundary scan test technology, and CAD technology. He was also responsible for the development of low power LSI technology, ASIC libraries, analog CMOS devices and SOI devices. From 1997 to 2003, he was a general manager in advanced LSI technology development center. On April 2003, he joined Tokyo Institute of Technology and he is a professor on physical electronics. Currently he is researching in mixed signal technologies, CMOS wireless transceiver, RF CMOS circuit design, data converters, and organic EL drivers.

He served as the guest editor in chief for special issues on analog LSI technology of IEICE transactions on electronics in 1992, 1997, and 2003, as the vice-program chairman for International Conference on Solid State Devices and Materials

(SSDM) in 1999 and 2000, as the Co-Chairman for Low Power Electronics Workshop in 1995, a member of program committee for analog technology in ISSCC and the guest editor for special issues of IEEE Transactions on Electron Devices. He has published 26 technical journal papers and 46 international conference papers. He is the co-author of 8 books. He holds 34 registered Japan patents and 65 US and EPC patents. He received the IR100 award in 1983, the R&D100 award and the remarkable invention award in 1994, and the ISSCC evening panel award in 2003 and 2005. He has been an IEEE Fellow since 2002.

Jan Sevenhans

Jan Sevenhans has served many years with ISSCC, first in the telecom subcommittee, later as European secretary, vice-chair and chair consecutively and this year as program chair. He is an IEEE Fellow. He worked on telecom circuits in Alcatel Antwerpen, Belgium from 1987 to 2003, after that in LEA Antwerpen for 2 years, and most recently in AMI Semiconductor in Vilvoorde, Belgium. His work was mainly for applications in GSM, ADSL, APON, ISDN, POTs, and on CMOS and bipolar silicon circuits and technology. He has filed many patents and published many articles in IEEE conferences and journals, and completed his Masters in 1979 at the K.U.Leuven in Belium. He was born in 1955 and completed his Masters in 1979 at the K.U.Leuven in Belgium. His Ph.D. in 1984 at the same university focused on the subject of CCD imagers for facsimile applications.

Leo Warmerdam

Leo Warmerdam received the MSc in Electrical Engineering from Technical University Delft, the Netherlands, and his Ph.D. in Technical Sciences from Technical University Twente, the Netherlands. During his Ph.D. he was visiting scientist at IMEC, Belgium, working on CMOS functions at cryogenic temperatures. In 1990 he joined Philips Semiconductors, where he worked on the introduction of high-voltage IC technology and associated designs for mains operated lighting systems and switched mode power supply (SMPS) applications. Warmerdam has worked on device physics and modeling, analog small signal and power design, high voltage electronics and power management functions.

From 1997 he was responsible for the product roadmap and market introduction of the GreenChip family of low power standby SMPS controllers. Next he led a team that worked on System-in-Package (SIP) concepts for high performance power converters for VRM and similar applications. In 2003 he joined Philips Research as department head of the analog and mixed-signal circuits and systems research group. His research interests include A/D and D/A conversion, highly digitized receiver architectures, digital calibration for analog circuits, high-speed data interfaces and power management.

Ian Young

Ian Young was born in Melbourne, Australia. He received the BSEE in 1972, and the M. Eng. Science in 1975, specialized in Microwave Communications, from the University of Melbourne. He received the Ph.D. in Electrical Engineering from the University of California, Berkeley, in 1978, where he was one of the pioneers of the switched capacitor filter in MOS technology.

In 1983 he joined the Technology Development group at Intel Corporation, where he is currently an Intel Senior Fellow and Director of Advanced Circuits and Technology Integration. His technical contributions have been recognized in the design of DRAMs and SRAMs, process technology development and microprocessor implementations, the design of Phase Locked Loops for microprocessor clocking and high speed I/O and mixed-signal RF CMOS circuits for communications.

He was a member of the Program Committee for the Symposium on VLSI Circuits from 1991 to 1996, serving as the Program Committee Co-Chair/Chairman in 1995 and 1996, and the Symposium Co-Chair/Chairman in 1997/1998. He currently serves on the Executive Committee of the VLSI Symposia. Since 1992 he has been a member of the ISSCC Technical Program Committee, serving as the Digital Subcommittee Chairman from 1997 through 2003, Technical Program Committee Vice-chair in 2004 and Chair in 2005. Dr Young is an IEEE Fellow.

New Conference Showcases the Young and Hot Digital Consumer Age in Asia

Nov 1-3, 2005 in Hsinchu, Taiwan

The inaugural Asia Solid-State Circuits Conference (A-SSCC) in Hsinchu, Taiwan on 1-3 November 2005 will target both business and academic interests with a selection of more than 100 talks and poster papers culled from over 350 submissions. These papers will report noteworthy advances in analog and digital, wireline and wireless circuit design, memory, frequency synthesizers, and system-level integration not only from Asia, but also from the rest of the world.The conference will also serve as a platform for international interaction.

Plenary Talks

To open the conference on Tuesday morning, Dr. Rick Tsai, CEO of TSMC, Taiwan will deliver a paper entitled "Design and Technology Collaboration." It will explore the methods and accomplishments of key collaborative initiatives at TSMC aimed at helping designers make the best use of technology to produce designs that are competitive in both performance and cost.

Immediately afterward, Dr. Ken Sakamura, of the University of Tokyo, will explain and portray the future of the "T-Engine." This collaborative product, consisting of a standard real-time "T-Kernel" running on standard hardware with networking facilities, uses nanoelectronics, software and embedded system technolo-


Dr. Rick Tsai


Dr. Ken Sakamura


Dr. Kinam Kim

gies to provide an open platform infrastructure for the embedded-system development of highly networked and high value-added products in a short period of time.

Wednesday's program will begin with a talk on semiconductor memory entitled "Memory Technologies for a Mobile Era," by Dr. Kinam Kim, SVP of Samsung Electronics.

He will describe how mobile appliances such as handheld phones, DCS's, and MP3's have recently driven the semiconductor business to devise non-volatile memories, especially mass storage NAND flash, to achieve increasingly longer battery-life and smaller and lighter packaging.

He will also explain how these requirements, plus the customer-orientation of mobile products and the ever-shortening product development life cycle, will continue to transform semiconductor memory from standard data storage to diverse memory solutions.

Pilot Industry Program

Specially featured on the first day will be a trial "Practical Industry Program," conceptualized by Dr. Nicky Lu and envisioned as a counterpart to the "Technology Directions" a component of the ISSCC. Product-based presentations about cutting-edge IC advances will be combined with specifications, applications, and live demos.

Tutorials

An all-tutorial program on Thursday will include four 90-minute talks scheduled sequentially so that all may be heard by the end of the day: "PLL/DLL," by C.K. Ken Yang of UCLA, "Analog Circuit Design Towards Nanometer Technologies," by Michiel Steyaert of K.U.Leuven, "Crypto Chip Design," by Cetin Kaya Koc of Oregon State University, and "High Performance DRAM Design," by Young-Hyun Jun of Samsung.

Panels

Panel Sessions on Tuesday afternoon will offer a choice between two topics:

Program details may be found at the conference web site: www.a-sscc.org.

"Wonder Drug for NRE Explosion: FPGA Reconfigurable Processor, Structured ASIC, SIP, or Conventional Approach?"

Non-Recurring Engineering cost for chip design is exploding. Design cost for chip and software is rapidly increasing. Only a handful of big projects can afford the conventional approach. Middle- and small-volume products may require a new solution. Could it be programmable commodity devices, such as FPGA and Reconfigurable Processor, or emerging ASIC devices, such as a structured ASIC? Or, could it be a SIP approach, where commodity chips rather than IPs are integrated in a package?

"What is the Best NV Memory for Portable Digital Consumer Applications?"

Portable applications require power-aware design, where Non-Volatile (NV) Memory is a key device. Recently, scaling Flash Memory to the next technology node has become increasingly difficult. The scaling challenges have motivated semiconductor memory makers to research and develop new NV Memories, such as FeRAM, MRAM, PRAM, and RRAM. Which is the most promising candidate to displace Flash Memory? Discussion shall be made for embedded and commodity use in the current and future markets.

Location

Nicknamed "the windy city" and famous for its special meatball and rice noodle delicacy, Hsinchu is first and foremost the site of the Hsinchu Science Park, Taiwan's "Silicon Valley," which was established in 1980 and housed a total of 384 high-tech companies by the end of 2004.

Takayasu Sakurai and the Steering Committee invite you to " . . . join the conference and feel the hospitality of Asia."

DAY	TIME SLOT	SESSION TITLE	SESSION TITLE	SESSION TITLE
Nov. 1, Tues	13:30-15:10	High-speed interconnects for system integration	Analog Signal Processing Circuits	Emerging Sensor and Control Systems
Nov. 2, Wed	10:00-11:40	Memory	Amplifiers	Emerging Integration and Voltage Conversion Techniques
Nov.2 Wed	12:40-14:20	Wireline communication Circuits	Frequency Synthesizers	Digital Circuits for Communication Systems
Nov. 2 Wed	14:55-18:00	Wireless Communication Circuits	VCOs and PLLs	High-performance Digital Circuits Design

Three simultaneous technical sessions in each of four time slots will highlight the topic as listed in this table.

Book Review: Delta-Sigma Data Converters

Breadth and Depth in Schreier and Temes' Comprehensive Book

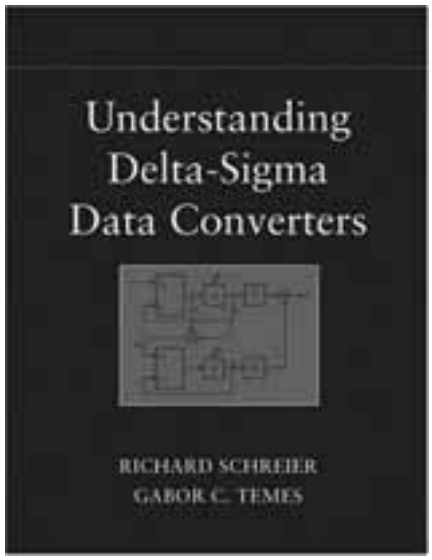
Reviewed by Ian Galton, University of California, San Diego, galton@ece.ucsd.edu
Understanding Delta-Sigma Data Converters
by Richard Schreier and Gabor C. Temes
Published by Wiley-IEEE Press in October '04, $89.95 ISBN: 0-471-46585-2

High-performance analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) based on delta-sigma modulation - collectively referred to as delta-sigma data converters - are enabling components in consumer communications and entertainment products including cellular telephones, wireless LANs, modems, mp3 players, and

AM/FM radios. They also represent an active area of research and innovation, driven by the ever-increasing performance demands of the consumer electronics marketplace, and the analog circuit design challenges imposed by the continued scaling of CMOS circuit technology. For example, in IEEE circuits conferences and journals alone, there have been over 1500 papers on the subject since 1962

Nevertheless, despite the intense industrial and academic interest in delta-sigma data converters, very few books have been written on the subject with both breadth and reasonable depth. This may be because relatively few authors feel qualified to write comprehensively on such a broad subject. The science of designing delta-sigma data converters is highly multi-disciplinary, drawing extensively on the fields of circuit design, signal processing, and communications theory. It is virtually impossible to design, or even understand, a high-performance delta-sigma data converter without a deep understanding of both theoretical and practical issues.

Until recently, academic papers, books on particular aspects of the field, and books consisting of chapters written by different authors have been the only means available to people wishing to gain a comprehensive understanding of delta-sigma data converters. A new book by Richard Schreier and Gabor Temes, Understanding Delta-Sigma Data Converters, Wiley-IEEE Press, 2005, is now is now available that addresses this problem. It provides a "one-stop shop" for engineers who want a comprehensive



introduction to the field of delta-sigma data converters. The authors are top researchers in the field with extensive industrial and academic experience in delta-sigma data converter design. They are also excellent teachers, with vast experience lecturing the fine points of delta-sigma data converter design to both university students and practicing engineers. As a result, the book is well polished, easy to understand, and provides a solid and broad introduction to the field.

Understanding Delta-Sigma Data Converters conveys the main ideas underlying delta-sigma data converters, i.e., oversampling and quantization noise shaping, at both an intuitive level and via mathematical analysis. The initial emphasis of the book is on simple, low-order delta-sigma modulation. It then builds on these concepts by explaining higher-order delta-sigma modulation, bandpass and quadrature delta-sigma modulation, dynamic element matching, and implementation considerations. The book nicely integrates the theoretical and practical aspects of delta-sigma data converter design. Numerous practical design examples are presented, and simulation techniques are covered in depth.

While no book on such a broad and rapidly evolving subject can be all-inclusive, Understanding Delta-Sigma Data Converters presents the core information and ideas underlying the field. The material it presents is essential background information for those wishing to understand the body of literature on delta-sigma data converters and those wishing to design delta-sigma data converters. It therefore provides an excellent starting point for engineers entering the field, as well as a useful reference for experts.

Most Downloaded CICC Article Features the Conference's Real-World Design Focus

Low-Voltage Low-Temperature-Coefficient CMOS Bandgap Voltage Reference

Kenneth S. Szajda, CICC Publicity Chair, kensz@sil.com

March is typically the month of most active Xplore usage, with over six million downloads, largely from regularly issued IEEE periodicals.

Philip T.K. Mok

Alex K.N. Leung

In 2005, fewer than 10% of those articles came from conferences. Yet "Design Considerations of Recent Advanced Low-voltage Low-temperature-coefficient CMOS Bandgap Voltage Reference" became one of the top one percent of downloads for the month, shortly after the CICC Digest was posted in Xplore.

This article examines the design considerations of CMOS bandgap voltage references, focusing on low-voltage and low-temperature-coefficient methodologies, and including the analysis of some recently reported circuits of bandgap voltage references. A CMOS voltage reference is also addressed.

It is enormously valuable to readers, principally because stable references are a key element in solid-state circuits. As more and more analog and digital functions are combined onto a single chip, one of the most signifi-

cant design challenges is realizing precision analog circuitry in a digital CMOS process. In the digital world, supply voltages have been shrinking in order to reduce power consumption, as feature sizes have been shrinking in order to increase density and performance. These factors in combination result in a widening of the PVT (process, voltage, and temperature) window, making precision analog design even more difficult.

Since the ability to generate precision reference voltages in a hybrid chip environment is key to achieving several key analog functions, especially D/A and A/D conversion in a digital process, Mok and Leung's findings have been of major interest.

DAC/ISSCC Student Design Contest Promotes Excellence

Founded in 1981 and incorporated into the International Solid-State Circuits Conference in partnership with the Design Automation Conference in 2002, the Student Design Contest has become a premier international competition for electronic systems designs prepared by graduate and undergraduate students as part of their studies. "Both DAC and ISSCC are the renowned conferences in IC design," said "Elvis" Pui-In Mak, a winner of last year's 42nd annual competition. "Their jointly held contest, therefore, can be considered the number one contest among all the others. Winners represent 'state-of-the-art' achievements in IC design."

Variety and Novelty

Contest projects encompass two categories: "Operational" designs that have been fabricated and tested, and "Conceptual" designs that have been simulated extensively and include test plans, but have not yet been fabricated or tested. The chief requirement for an operational design is the inclusion of "measurements demonstrating that it works as expected," said David Greenhill, a 2004 contest co-chair. The criteria for a conceptual design are "based on simulation and a plan for how the design will be tested if and when it is built."

Mr. Greenhill praised the "very wide range of different design styles" submitted for competition. The biggest challenge for the judges is the breath of papers," he said. "Somehow they have to compare apples and oranges and decide which are best." The most fun for the judges is being exposed "to what is being designed in Academia. A lot of new and novel ideas come out of this. It definitely makes the judges think outside of their day to day design box."

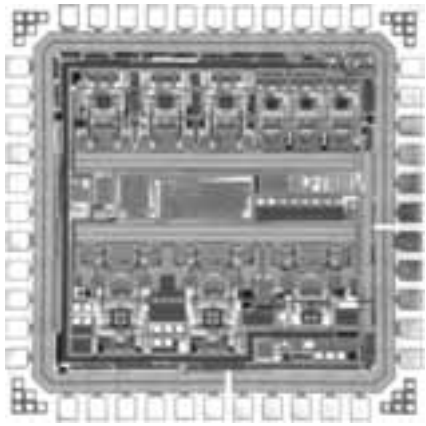
Imran Ahmed of the University of Toronto who, with David Johns, was the Overall and Operational Category winner last year, thought the competition helped advance his academic goals. "The process of putting together a submission has a 100% return in aiding one to further develop their research writing/presentation skills," he said. "In addition, the design contest process is a nice way to become familiar with the publications process."

Cash Prizes

Contestants vie for prizes donated by the Conferences and by industry supporters, including the Association of Computing Machinery (ACM) Special Interest Group on Design Automation (SIGDA), the Microelectronics Advanced Research Corporation (MARCO) and the Semiconductor Research Corporation (SRC) in 2004. Prize winners show their work at the annual DAC meeting in June and at the ISSCC in San Francisco in February. "If there is one thing that always makes a graduate student happy," Mr. Ahmed said, "it's money, which makes winning the $5,000 prize money the best part of the experience. Having a reason to legitimately take time during school to go visit California comes a close second."

Networking

The best part of the whole experience, Elvis Mak said, was the opportunity to meet and share ideas with admired researchers. "Many experts in related fields expressed an interest in our work and provided important comments during the discussion. It was my good fortune to meet face to face with some professors and researchers whose papers I had only been able to read, and see their photos in the JSSC."



Winners of the 42nd Annual Student Design Contest

OPERATIONAL CATEGORY

1st Place (Best Overall) A 50MS/s (35mW) to 1kS/s (15 É W) Power Scaleable 10b Pipelined ADC with Minimal Bias Current Variation. Imran Ahmed, David Johns - Univ. of Toronto, Toronto, ON. Canada

2nd Place A 1.3 TOPS H.264/AVC Single-Chip Encoder for HDTV Applications. Tung-Chien Chen, Yu-Wen Huang, Chen-Han Tsai, Ching-Yeh Chen, To-Wei Chen, Liang-Gee Chen - National Taiwan Univ., Taipei, Taiwan

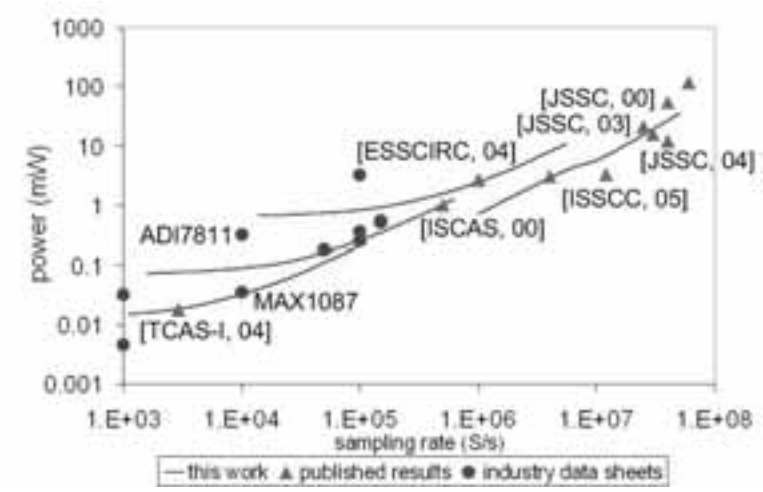
3rd Place A Side-Channel Leakage Free Coprocessor IC in 0.18É m CMOS for Embedded AES-based Cryptographic and Biometric Processing. Kris Tiri, David Hwang, Alireza Hodjat, Bo-Cheng Lai, Shenglin Yang, Patrick Schaumont, Ingrid Verbauwhede - Univ. of California, Los Angeles, CA

STUDENT DESIGN CONTEST DUE BEFORE 5 pm MST, Dec. 6, 2005

Students are invited to submit descriptions of original electronic designs, either circuit level or system level. Student Design Contest paper submissions must (1) be in PDF format only, (2) contain the title of the project, (3) contain an abstract of approximately 60 words, (4) contain a complete description of the project, and (5) be no more than 6 pages (including the abstract, maximum of 10 figures/tables and references), double-columned, 9pt or 10pt font. The submission should clarify the originality, distinguishing features, and measured performance of the design. Two categories of designs - operational and conceptual - are eligible for awards. For operational designs, proof-of implementation is required, while for conceptual designs, complete simulation is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2004. Submitted designs should not have received awards in other contests. Selected designs will be presented at the conference (and at ISSCC in February 2006). Additional submission guidelines are available on the DAC web site.

2005 Contest Chairs: Alan Mantooth (University of Arkansas) and Bill Bowhill (Compaq Computer Corporation)

More information may be found at: www.dac.com "Call for Papers"



From "A 50MS/s (35mW) to 1kS/s (15É W) Power Scaleable 10b Pipelined ADC with Minimal Bias Current Variation," by Imran Ahmed and David Johns - Univ. of Toronto, Toronto, ON. Canada, providing a comparison of their results with industry data sheets.

CONCEPTUAL CATEGORY

1st Place Design and Implementation of a Fractional-N Frequency Synthesizer for Cellular Systems. Petrus J. Venter, Saurabh Sinha - Univ. of Pretoria, Pretoria, South Africa

2nd Place A 1-V IEEE 802.11a/b/g-Compliant Receiver IF-to-Baseband Chip in 0.35É m CMOS for Low-Cost Wireless SiP. Pui-In Mak, Rui P. Martins - Univ. of Macau, Macao SAR, China. Seng-Pan U - Chipidea Microelectronics (Macau) Ltd., Macao SAR, China

3rd Place Collision Detection System using an FPGA Implemented on the FPX Platform. Hasan N. Atay, Burchan Bayazit, John W. Lockwood - Washington Univ., St. Louis, MO

Advice to Applicants

"The key aspect to a successful submission," Mr. Ahmed said, "is to carefully organize and write your submission in such a way that a person who does not know anything about your work will get enough basic ideas out of it that they will want to read more about it, either through your thesis or published papers. Trying to explain every small detail complicates the discussion and distracts the reader from the key points you have. However, to make your paper also appealing to experts in your field, you should provide a concise summary of your results and, most importantly, compare against previous works to put your work in context,"

FOR INFORMATION CALL: 1-303-530-4333

Call for Fellow Nominations

Being named an IEEE Fellow is a lifetime honor. It is recognized and respected by your colleagues throughout the industry. It is recognition for major technical contributions. Many Fellows add the title to their business cards.

The Fellow nomination form is four pages long. The nominator does not have to be an IEEE Fellow or even an IEEE member. It is not difficult to complete and should focus on the technical achievements of the nominated candidate. Self-nomination is not allowed; however, collaboration between nominator and candidate is almost universal. A minimum of five and a maximum of eight references are required from current IEEE Fellows. A complete list of IEEE Fellows is available on line at:

www.ieee.org/portal/pages/about/awards/fellows/complete-list-ieee-fellows1.html

The deadline for receipt of the nomination form and reference letters is March 2006. This is an absolute deadline!

Being an IEEE Senior Member, is a prerequisite for Fellow elevation. The Senior Member application process and its supporting references must be completed and evaluated successfully prior to a Fellow application being considered. There are Senior Member Review Panels meeting in September, November, and January, so now is a good time to begin the Senior Member application process. Senior Member forms can be completed online or forms can be downloaded in a number of formats at the URL: www.ieee.org/organizations/rab/md/smguide.html

Make this year a year in which you are involved in an IEEE Fellow nomination. It is an honor which the leaders of our profession deserve.

Fellow nomination kits for the class of 2007 will be available in September and can be downloaded from the Web URL: www.ieee.org/portal/pages/about/awards/fellows/request.html

How to Become a Senior Member

Among the benefits of IEEE Senior Membership is the professional recognition of your peers for technical and professional excellence. SSCS announces the list elevated members in the Society newsletter each issue. Senior Membership is also a prerequisite to the Fellow nomination process. There are certain executive IEEE volunteer positions for which one must be a Senior Member to be eligible. Only Senior Members/Fellows can serve as references for colleagues who apply for Senior Member. IEEE provides an attractive fine wood and bronze, engraved Senior Member plaque to display. New senior members receive up to $25.00 as a gift certificate toward one new Society membership. A letter of commendation to one's employer on the achievement of Senior Member grade is sent if requested by the new Senior Member.

If you meet the requirements, you should apply. IEEE Bylaws state the criteria for elevation to Senior Member Grade: "... a candidate shall be an engineer, scientist, educator, technical executive or originator in IEEE-designated fields. The candidate shall have been in professional practice for at least ten years and shall have shown significant performance over a period of at least five of those years."

The Admission and Advancement Committee evaluating your application will count the years you have been in professional practice. Your educational experience is credited toward that time as follows:

- 3 years for a baccalaureate degree in an IEEE-designated field
- 4 years if you hold a baccalaureate and masters degree
- 5 years if you hold a doctorate

The Senior Member application form is available in 3 formats: an online version for direct submission, a downloadable pdf version to print and complete and electronic version where information can be entered, saved and submitted as an e-mail attachment. For forms, schedule of review panel meetings, and other information about the process are available online.

www.ieee.org/organizations/rab/md/smprogram.html

Chapter Activities Feature Guest Speakers from Industry, Government and Academia

Zurich Chapter Hosts ESD Protection Circuitry Lecture

Markus Helfenstein , Philips Semiconductor, markus.helfenstein@philips.com

The IEEE SSCS Zurich Chapter and Philips Semiconductors, Zurich jointly organized a lecture on the design of ESD protection circuitry. The IEEE distinguished lecture entitled "Mixed-Mode ESD Protection Circuitry Design for RF/M-S ICs: Prediction and Characterization" was given by Prof. A. Wang, Faculty of ECE, Illinois Institute of Technology, USA.

About 100 people from both industry and academia attended this seminar, which was held on the Philips premises. In this lecture, Prof. Wang discussed a CAD-based mixed-mode ESD simulation-design methodology that enables ESD protection design prediction for mixed-signal/RF applications. Critical characterization techniques for mixed-signal/RF ESD protection design were presented as well as practical ESD protection circuit design examples. This seminar received many positive comments.

Students at Novosibirsk University Expand Chapter Projects

Members of the Novosibirsk State Technical University Student Chapter donated technical support to the 6th Annual International Siberian Workshop and Tutorial on Electron Devices and Materials (EDM 2005), which took place in July at the University, and prepared its Proceedings in hardcover and on CD. The group similarly contributed technical expertise to the 5th International Microwave Electronics: Measurements, Identification, Application Conference (MEMIA 2005), in collaboration with its dynamic parent organization, the IEEE Novosibirsk Joint ED/MTT/CPMT/COM/SSC Chapter. Together, they are establishing a website (http://www.nstu.ru/edm) to make the papers presented at EDM 2005 available to the public.

With the aid of SSCS subsidies for 2005, the Chapter established a Student Branch Library and CADFEM Laboratory, and renovated the Student Branch Web site. It is now being reconstructed and will be restored in September.

Prof. Albert Wang (right) and Dr. Markus Helfenstein (organizer, Philips Semiconductors Zurich) exploring the old town of Zurich.

DM2005 available to the public. (http//www.nstu.ru/edm)

In 2006-2007, the Chapter looks forward to establishing new CAD Laboratories, launching a Student Paper Award, recruiting new members, and forming other Student chapters in the Siberia region under the direction of a newly elected Executive Committee. The group's long-range goals are to expand local student activity in SSCS/EDS content areas by means of the facilities it has already set up, and through presentations, seminars, social events, exhibitions, interviews and periodicals.

Nataliya V. Hainovskaya, IEEE/EDS Student Chair; Artem E. Nastovijak, IEEE Student Branch Secretary/Treasurer; Alexander V. Gridchin, IEEE Student Branch Counselor; Victor A. Gridchin, IEEE SSCS Student Branch Chapter Advisor, Dr. Sc., Prof., Head of Dept. of Semiconductor Devices and Microelectronics of Novosibirsk State Technical University

Denver Chapter Broadcasts Seminars Using WebEx and Audio-Conferencing

During the past four months, the SSCS Denver Chapter, based in Fort Collins, hosted four technical meetings, including three Distinguished Lecture seminars, and a BBQ social.

"We continue to promote technology-related topics in hopes of educating the local design community about the ever-growing importance and complexity of technology and reliability considerations in deep submicron CMOS design," said Chapter Chair Alvin Loke. "In an attempt to reach interested out-of-town participants, we started making seminars available via WebEx and audio-conferencing. In our pilot attempt, folks signed in from Houston, Santa Clara, Palo Alto, and even Singapore!"

"We look forward to growing participation in upcoming seminars," Dr. Loke said. "Please visit ewh.ieee.org/r5/denver/sscs/ for more information about our chapter events."

In April, Jeff Rearick of Agilent Technologies presented a tutorial on "Analog Adventures in Digital Chip Testing." It focused on analog issues and considerations in high-speed digital production testing, and also touched on incorporating embedded test capability as an emerging SoC trend.

During July and August, Denver had the honor of hosting three Distinguished Lecturers:

First, Prof. Jan Van der Spiegel, SSCS Chapters Committee Chair, who visited from the University of Pennsylvania, delivered a fascinating seminar on "Biologically Inspired Smart CMOS Vision Sensors." This seminar was jointly held with the Chapter's Centennial Section in order to grow awareness of chapter activities beyond SSCS membership.

Then the Chapter was privileged to have Prof. Jack Lee, from the University of Texas at Austin, deliver an informative talk on "High-K Gate Dielectrics," a key development for 45nm high-performance CMOS. Finally, Prof. Dieter Schroder, from Arizona State University visited Fort Collins to speak on"Negative Bias Temperature Instability (NBTI)." He highlighted circuit implications and workarounds, and elucidated the physical origins of NBTI.

July Denver Chapter meeting with officers from the Centennial Subsection of the Denver Section. The Centennial Subsection encompasses Fort Collins one hour north of Denver. L to R: Bob Barnes (Treasurer), Tin Tin Wee (Secretary/Webmaster), Alvin Loke (Chair), Prof. Jan van der Spiegel (SSCS Chapters Committee Chair), Pete O'Neill (Centennial Program Director), Ron Peiffer (Centennial Treasurer), Osvaldo Buccafusca (Centennial Vice Chair)

Baltimore Joint Chapter Featured Three Guest Speakers in 2004-2005

James Oliver, Chapter Chair, james_oliver@ieee.org

The SSCS/Electron Devices Baltimore joint chapter held three technical meetings featuring outside speakers during its 2004-2005 season.

The first two presentations on electron devices comprised papers entitled "Microsystems Enabling System Innovation," by John Zolper of DARPA, and "GaN-based Field Effect Transistors," by Electron Devices Society Distinguished Lecturer Prof. Michael S. Shur of Rensselaer Polytechnic Institute.

A third paper, addressing solid-state circuits interests, was "An Overview of MOSFET Device Behavior and Modeling for Mixed-signal/RF IC Design," by Electron Devices Society Distinguished Lecturer Dr. Yuhua Cheng of Siliconlinux, Inc.

Meetings of the SSCS/ED Baltimore joint chapter are held at the Historical Electronics Museum in Linthicum, MD. They are open to the public without cost, and provide IEEE brochures and enrollment information to non-members. To publicize its activities, the Baltimore Chapter maintains its own website, which can be accessed directly at ewh.ieee.org/r2/baltimore/edssc/index.html, or indirectly via the "Chapters-Technical" hyperlink of the Baltimore section site.

SSCS Newsletter July e-News Features

The SSCS Newsletter is printed 3 times a year, and alternate months throughout the year e-news is posted with alerts sent by email. Here are topics posted in the July e-news.

- Jack Kilby, Pioneer of an Industry continues to inspire lives.
- ESSCIRC 2005 to be held in Grenoble in September
- CICC Celebrates 27 Years of Innovation, Education and Communication
- Low Power Symposium Celebrates Tenth Anniversary
- Chapters Report: Bangalore and joint Yugoslavia
- Consumer Tip: Deciding the Better Subscription Deal
- Technology Worth Reading
- IEEE 2006 President-Elect Candidates Field Questions

To review issues online selected e-news Archive from the home page of the SSCS e-news.

www.ieee.org/portal/site/sscs

To receive the November SSCS e-news, which will not be available in print, please request to join the list at www.ieee.org/ra/e-notice/sscs-enotice.html

Online IEEE Member Renewal is Easy

Over the last 5 years a growing number of IEEE members are renewing on line. More than 60% of members are expected to renew online this year. The look and feel of the renewal screens have been streamlined this year. Logon and see how simple it is. http://services1.ieee.org/membersvc/member/sscs_intro.htm

Because 95% of IEEE student members renewed online last year, this fall all student renewals will be online, and there will be no postal mail used at all. Students will receive an email alert the first week of October explaining the new system. Two days later an encrypted pdf file of all their existing membership information and subscriptions will be sent by email, with their unique member number as the password to open the file. Instructions will direct students to renew online.

Regular membership renewal reminders, mailed the first week of October, will take two forms. For all Life members and for other members who have never renewed on line, a full packet will be sent, just as a decade ago, with a covering letter, an invoice, a second copy of the invoice to keep for personal records, a pamphlet describing all Society and all publication offerings, and a return envelope.

For members who have renewed or joined online already, a packet will be sent that includes a covering letter and invoice but no return envelope or detailed pamphlet. Information about Societies and publications are online along with the renewal web pages. 60% of IEEE members will receive this lighter mailing for renewal online. At 1/3 the weight of the full package, it will reduce the costs of printing, paper and mailing by well over half.

SSCS dues, which include access to the JSSC through Xplore, are the same $18 as last year, while the print JSSC is now $20. The JSSC has increased page rate from 1,930 in 2002, to 2,584 in 2004, with expected 2,700 pages scheduled for 2006. At $20, the JSSC print subscription is the most-read yet least expensive monthly technical journal offered by IEEE.

Other SSCS subscription renewal offerings

-- CD of the JSSC articles of the last two years for $30.

Mailed in late spring of 2006, this CD of 2004 and 2005 articles will include indices of all years of the Journal plus four key solid-state conferences.

a) ISSCC, International Solid-State Circuits Conference from 1955 to 2005
b) VLSI, Symposium on VLSI Circuits 1988 to 2005
c) CICC, Custom Integrated Circuits Conference 1988 to 2005
d) ESSCIRC, European Solid-State Circuits Conference 1997 to 2005.

The pdfs of the conference articles are not on the CD but are available online and on the SSC Archive DVD described below; the index on the CD allows searching untethered.

-- The Conference Digital Library for $75.

This annual subscription allows access through Xplore to all the articles in pdf of the conferences listed above. Most SSCS articles are posted about 6 months after the conference occurs.

-- The New Journal of Display Technology for $26 online.

See the table of contents of the September first-issue posted online. For 2006 the JDT goes to quarterly publication. This Journal's rates are $26 for online, $28 for print, and $39 for both in 2006

Sscs.org/pubs/j-dt.htm

SSC Digital Archive 2004 -- DVD pair

The SSC Digital Archive is available as a special purchase not through subscription at renewal time. It contains the complete collection of all the articles in pdf, from the 4 four key solid-state conferences and all JSSC articles from 1966 through 2004. A bonus index is included on the disk set, of key publications in the field of Electron Devices. Priced at $150 for members, the DVD pair can be ordered directly through this URL.

shop.ieee.org/ieeestore/product.aspx?product_no=JD3755C

To read more about this disk Archive see the March 2005 SSCS e-news article "2004 SSCS Digital Archive DVD Issued"

www.ieee.org/portal/pages/sscs/05Mar/04DVDpair.html

SSCS EVENTS CALENDAR

Also posted on *www.sscs.org/meetings*

SSCS SPONSORED MEETINGS

2005 CICC Custom Integrated Circuits Conference
www.ieee-cicc.org
18–21 September 2005
San Jose, CA, USA
Paper deadline: passed
Contact: Ms. Melissa Widerkehr, cicc@his.com

2005 A-SSCC Asia Solid-State Circuits Conference (the first meeting)
www.a-sscc.org/
1–3 November 2005
Hsinchu, Taiwan
Paper deadline: passed
Contact: org@a-sscc.ee.ntu.edu.tw

2006 ISSCC International Solid-State Circuits Conference
www.isscc.org
5–9 February 2006
San Francisco Marriott Hotel, San Francisco, CA, USA
Paper deadline: 15 September 2005
Contact: Courtesy Associates, ISSCC@courtesyassoc.com

2006 Symposium on VLSI Circuits
www.vlsisymposium.org
15–17 June 2006
Honolulu, Hawaii
Paper deadline: 8 January 2006
Contact: Phyllis Mahoney, vlsi@vlsisymposium.org
or Business Center for Academic Societies, Japan, vlsisymp@bcasj.or.jp

SSCS TECHNICAL CO-SPONSORED MEETINGS

2005 European Solid-State Circuits Conference
www.esscirc2005.org/
12–16 September 2005
Grenoble, France
Paper deadline: passed

2005 Bipolar/BiCMOS Circuits and Technology Meeting
www.macs.ece.mcgill.ca/~rfic/bctm05/index.htm
9–11 Oct 2005
Santa Barbara, CA
Paper deadline: passed

2005 Compound Semiconductor IC Conference
www.csics.org/
30 Oct – 02 Nov 2005
Palm Spring, CA
Paper deadline: passed

2005 International Conference on Computer Aided Design
www.iccad.org
6–10 November 2005
San Jose, CA, USA
Paper deadline: passed

2006 International Conference on VLSI Design
www.isical.ac.in/~vlsi2005
3–7 January 2006
Hyderbad, India
Paper deadline: passed

2006 Asia and South Pacific Design Automation Conference
www.aspdac.com/aspdac2006/
24–27 January 2006
Yokahama City, Japan
Paper deadline: passed

2006 Design, Automation and Test in Europe
www.date-conference.com/conference/next.htm
6–10 March 2006
Munich, Germany
Paper deadline: 11 Sep 2005

2006 Radio Frequency Integrated Circuits Symposium
www.rfic2006.org
11–13 June 2006
San Francisco, CA, USA
Summary deadline: 2 Jan 2006

2006 Symposium on VLSI Technology
www.vlsisymposium.org
13–15 June 2006
Honolulu, Hawaii
Paper deadline: 8 Jan 2006

2006 Design Automation Conference
www.dac.com
24–28 July 2006
San Francisco, CA, USA
Paper deadline: TBD

IEEE SOLID-STATE CIRCUITS SOCIETY NEWSLETTER is published three times per year, January, May, and September by the Solid-State Circuits Society of The Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. $1 per member per year (included in society fee) for each member of the Solid-State Circuits Society. This newsletter is printed in the U.S.A. **Postmaster:** Send address changes to IEEE Solid-State Circuits Society Newsletter, IEEE, 445 Hoes Lane, Piscataway, NJ 08854.

To maintain all your IEEE and SSCS subscriptions, email address corrections to *address-change@ieee.org*
To make sure you receive an email alert, keep your email address current at *sscs.org/e-news*

445 Hoes Lane
Piscataway, NJ 08854

Non-Profit Org.
U.S. Postage
Paid
Easton, PA
Permit No. 7