# A 50MS/s (35mW) to 1kS/s (15μW) power scaleable 10b pipelined ADC with minimal bias current variation

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## ABSTRACT
A new opamp with a short power on time, and a current modulation technique, are used to implement a 10b 1.5b/stage pipelined ADC (in 0.18μm CMOS) which has a scaleable power between 1kS/s (15μW) and 50MS/s (35mW), while only varying the bias currents by a factor of 50. An SNDR of 54-56dB was measured for all sampling rates.

## Keywords
ADC, Analog, Power scaleable, CMOS, low power, Student submission

## 1. INTRODUCTION
ADCs having a power that scales with sampling rate can significantly reduce manufacturer costs, as a single ADC can be used to target multiple applications with different performance requirements - reducing development costs, and time to market. Low power applications requiring multiple operating speeds and multiple standard compliancy (e.g.: mobile, biomedical) also benefit from a single ADC with scaleable power. The power of CMOS digital circuits explicitly scales with sampling rate according to $0.5fCV^2$. ADC power however is dominated by analog power, which does not explicitly scale with sampling rate. Previous publications of high speed ADCs achieve scaleable power by making opamp bias currents a function of sampling rate. In [1] opamp bias currents were varied by 1:1000 to scale power between sampling rates of 20kS/s-20MS/s in a 10b pipeline/delta-sigma ADC. In [2] Opamp bias currents were varied to reduce ADC power between 3MS/s (~12.5mW) to 220MS/s (135mW), for a power scaleable range of 1:11 over a sampling rate variation of 1:73. Extended bias current variations to maximize the power scaleable range however forces current mirrors into weak inversion, resulting in reduced accuracy and yield, increased sensitivity to noise, and increased design and verification time due to multiple design corners. In this paper, a 10b 50MS/s 1.5b/stage pipelined ADC in 0.18μm CMOS is presented which by using a current modulation technique and a novel rapid power-on opamp, enhances the power scaleable range of current scaling by 50x, allowing for wide variations in sampling rate and thus power, with minimal variations in bias current. This is the first known published [3] high speed ADC to achieve a power scaleable range as large as 1:2500, while only relying on a minimal amount of bias current variation of 1:50.


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## 2. STRONG VS. WEAK INVERSION
MOS transistors operate approximately in strong inversion when $V_{eff}=V_{GS}-V_t>200mV$, and approximately in weak inversion when $V_{eff}<-70mV$ [4]. A lower biasing current results in smaller $V_{eff}$. In ADCs using frequency dependent biasing, for large sampling rate variations, transistors can become biased in weak inversion for low sampling rates. The rate of change of drain-source current ($I_{DS}$) with gate-source voltage is given approximately as:

$$\frac{dI_{DS}}{dV_{GS}} \propto (V_{GS}-V_t) \quad \text{for strong inversion, and}$$

$$\frac{dI_{DS}}{dV_{GS}} \propto e^{\frac{V_{GS}-V_t}{nU_T}} \quad \text{for weak inversion.}$$

Thus if a transistor in weak inversion acts as a current source to an opamp, a very small variation of the current source's gate-source voltage due to (e.g.) noise coupling from a nearby digital circuit, or threshold mismatch, can cause opamp bias currents, thus bandwidth to fluctuate significantly (>30% for 3 sigma of total yield [5]). Since the settling accuracy of a sample and hold is a strong function of opamp bandwidth, current mirrors in weak inversion result in ADCs with highly sensitive settling accuracies. Furthermore as the transistor enters weak inversion, $V_{GS}$ becomes very small, reducing the relative magnitude of $V_{GS}$ to fixed noise and/or offset, i.e. the SNR of the bias voltage decreases. The combination of these drawbacks results in weak inversion designs generally having poorer yield [5], thus being more costly to design, verify and test – significant disadvantages in industrial applications. For this work to improve on the drawbacks of previous designs, the ADC of this work must have a very wide power scaleable range on the order of previous publications [1], [2], but with a significantly lower dependency on bias current scaling.

## 3. ARCHITECTURE OVERVIEW
In digital circuits power is typically consumed on output transitions where only enough power is consumed to set the digital output to the desired logic level. A characteristic of an ADC which may be exploited is although ADCs are predominantly

analog, the final output is digital. Thus per output sample, the ADC only requires enough power to set the ADC output to the correct logic levels representing the analog input. When an ADC operates at full speed, just enough analog power is supplied to allow the analog circuits to settle to the desired accuracy, and thus provide the correct digital output. If however bias currents are unaltered while ADC sampling rate is decreased, the settling time ($t_{settle}$) of analog blocks in an ADC becomes a smaller percentage of the period. Thus if the digital outputs of the ADC are latched after $t_{settle}$, and the ADC powered down after $t_{settle}+t_{latch}$ ($t_{latch}$ is the time to latch the digital output) as shown in Figure 1, the ADC will have an average power of: $P_{avg}=P_{ON}t_{ON}f_s$ ($t_{ON}=t_{settle}+t_{latch}$; $P_{ON}$ is the ADC power consumed during $t_{ON}$). With this approach, lower power for lower sampling rates is achieved by only changing the time the ADC is off ($t_{OFF}=T-t_{ON}$), and without adjusting bias currents, thus low power and strong inversion performance can be retained for low sampling rates. In fact, the lowest power achievable with this Current Modulated Power Scale (CMPS) approach is limited only by blocks that consume non-zero average power during $t_{OFF}$. The highest sampling rate attainable with CMPS is limited by how quickly the ADC can power on from a state of minimal power consumption during $t_{OFF}$, which is the key design challenge of this work.

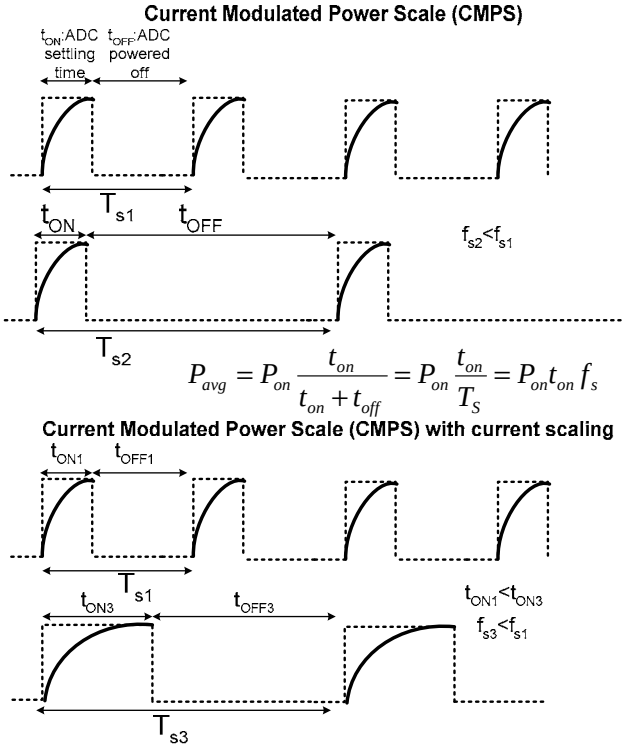


**Figure 1. Current Modulated Power Scale (CMPS)**

If bias currents are scaled, CMPS enhances the power scaleable range of current scaling (Figure 1). For example, if current scaling is used to vary ADC power by 1:10, and CMPS allows ADC power to be reduced by 1:50, application of CMPS to the lowest power achievable with current scaling results in a minimum power of $1/(10 \times 50)=1/500^{th}$ the maximum power. Thus the CMPS architecture necessarily improves on any previous architecture which relies on current scaling alone to achieve power scaleability. The lowest power achievable with CMPS + current scaling is limited practically by how much current scaling can be tolerated by the application in question.

CMPS can be applied to any Nyquist rate ADC architecture to achieve scaleable power with sampling rate. The ADC architecture chosen for this work was a 1.5b/stage 10b pipeline. The pipeline architecture is capable of moderate to high speed accuracy and sampling rate, thus is used in many applications. 1.5b/stage were used, as redundant bits relax the matching constraints of the ADCs found in each stage of the pipeline. As key previous publications [1], [2] of power scaleable ADCs were 10b 1.5b/stage pipeline architectures, implementing the same architecture also allows for a fair comparison of measured results. A maximum sampling rate of 50MS/s was chosen to demonstrate the feasibility of the CMPS architecture at high sampling rates.

With CMPS applied to a pipeline architecture, after an input is digitized all pipeline stages are powered down, thus are reset. Hence when the ADC is powered on again, the next digital output is available only after the sampled analog input traverses the entire pipeline. That is $t_{ON}$ equals the latency of the ADC ($t_{lat}$). Thus the maximum sampling rate when using CMPS on a pipeline ADC is $1/t_{lat}$, which is lower than $1/t_{stage\text{-}lat}$ - the maximum sampling rate of achievable with a pipeline ADC (where $t_{stage\text{-}lat}$ is the maximum latency of a single pipeline stage). To achieve scaleable power for sampling rates not allowable with CMPS enabled (i.e. between $1/t_{lat}$ and $1/t_{stage\text{-}lat}$), the ADC is operated as a conventional pipeline ADC (i.e. CMPS disabled), where current scaling is used to achieve scaleable power for the narrow range of non-CMPS sampling rates. Through careful design, the transistors can avoid operating deep in weak inversion over the narrow current scaling range ($t_{atage\text{-}lat}$ : $t_{lat}$) required. A block diagram of the overall power scaleable ADC is shown in Figure 2.

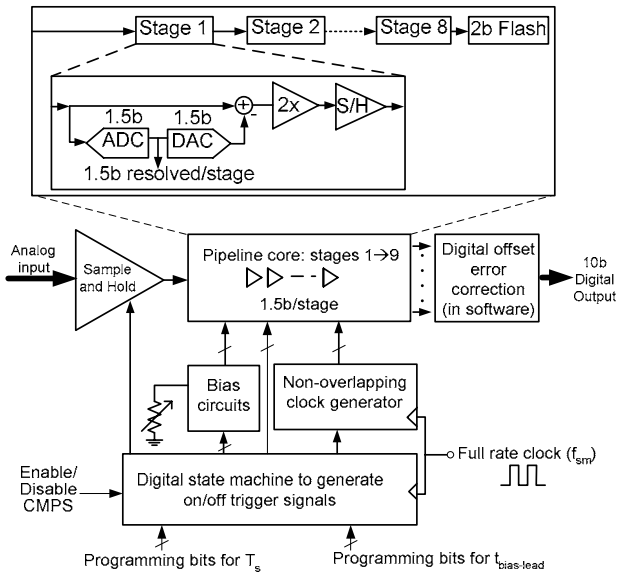


**Figure 2. System Level diagram of Pipelined ADC**

External control bits are used to enable/disable CMPS, and a constant current biasing scheme with a tunable external reference current used to set the on chip bias currents. When CMPS is enabled, only one pipeline stage is powered on at a time to save power as shown in Figure 3, as only one analog sample is digitized every $T_s$ (i.e. the ADC operates similar to an algorithmic ADC). Before each stage is powered down, its digital output is latched.

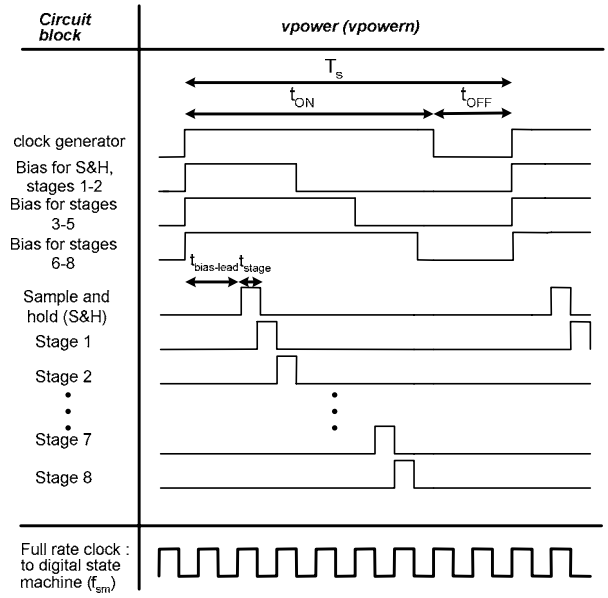


**Figure 3. Power on/off timing of blocks in ADC**

# 4. ADC IMPLEMENTATION

As shown in Figure 2, the pipeline core consists of an ADC, DAC, 2x gain, and Sample and Hold (S/H). The DAC, 2x gain, and S/H are lumped into a single circuit referred to as the Multiplying Digital to Analog Converter (MDAC). The following sections detail the implementation of each block in Figure 2.

## 4.1 Stage ADC

Digital error correction is commonly used in pipeline ADCs to relax the matching constraints of comparators in the stage ADC, such that comparator offset can be as high as $V_{FS}/4$ (where $V_{FS}$ is the single-ended full scale voltage of the input). Dynamic comparators were used to implement the stage ADC as less power is consumed than active comparators, and have the advantage of only consuming power during output transitions. Low power Lewis and Gray comparators [6] have been used in previous publications to implement the dynamic comparator. Monte Carlo simulations of the Lewis and Gray comparator in a 1.8V 0.18µm CMOS process however show a normally distributed offset, with $3\sigma$=282mV. With $V_{FS}$=0.8V to ensure reliable operation over process and temperature corners, the maximum comparator offset allowable was 200mV. To ensure a high yield, the lower offset but higher power charge sharing dynamic comparator (Figure 4) was used, which was found through Monte Carlo simulations to have a normally distributed offset of $3\sigma$=54mV. The threshold of the ADC was set by the ratio of sampling capacitors [6].

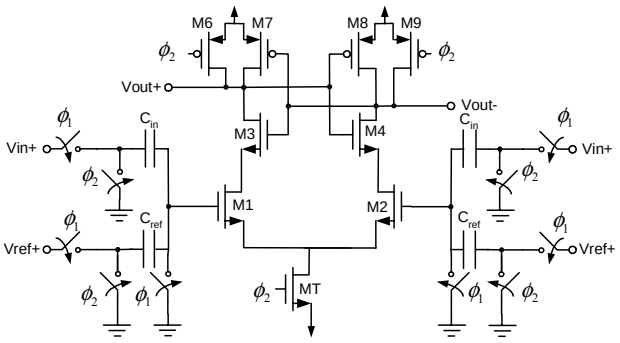


**Figure 4. Charge Sharing Comparator for stage ADC**

## 4.2 Stage MDAC/Front end sample and hold

A commonly used MDAC architecture [7] was used in this work, and is shown in Figure 5 (shown single ended, but implemented differentially to reject common mode noise and odd order harmonic distortion [8]). The MDAC architecture has a large feedback factor, hence fast transient response [8], and good matching (due to identical capacitor sizes). Capacitor sizes for $C_1$=$C_2$ were 500fF, 100fF, and 50fF for stages 1-2, 3-5, and 6-8 respectively. Capacitors were sized and verified in Matlab, such that the thermal noise due to sampling [8] contributed to a random error of less than a quarter LSB. SPICE simulations were used to determine optimal switch sizes for the MDAC, such that the maximum RC time constant was sufficiently small to allow for a maximum sampling rate of 50Msps.

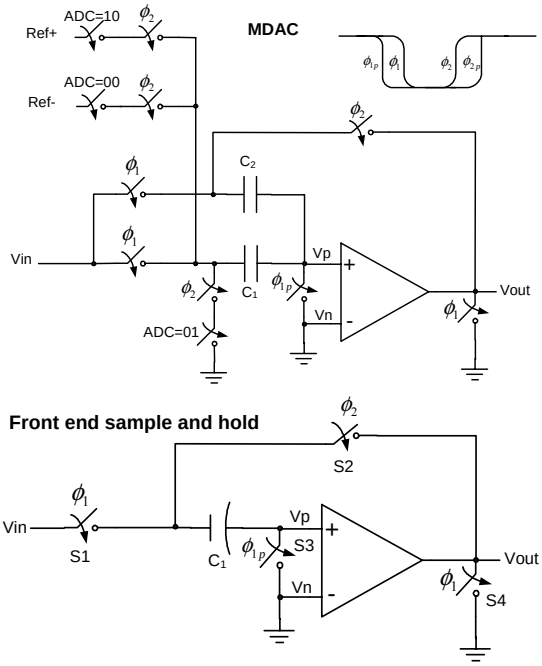


**Figure 5. Stage MDAC, Front end Sample and hold**

A popular sample and hold architecture [7] was used before the first stage in the pipeline (Figure 5). A front end sample and hold,

eliminates sampling skew between the first stage MDAC and ADC. Previous publications have shown a mix of ADCs with and without a front end sample and hold for sampling rates on the order of 50MS/s. In the interest of a higher likelihood of functionality, and a more relaxed layout, a front end sample and hold was used at the penalty of increased power consumption.

## 4.3 MDAC/Sample and Hold Opamp

The key challenge in this work for high speed operation is to be able to rapidly power on/off the opamps and their bias circuits according to the timing of Figure 3. Opamps which power on/off are seen in previous literature in the form of switched opamps [9], where opamp bias currents are modulated by switching current source bias voltages. Bias voltage switching however results in slow opamp power on time, as switched bias voltages are required to slew [10] to reach the steady state bias voltages during $t_{ON}$. Furthermore, since large capacitors are often used on bias nodes to minimize the effects of noise, the bias slew rate is very low.

In this work, a novel replica bias technique was developed and is used to rapidly power on/off MDAC opamps completely (Figure 6). Switching a copy of the bias voltage to an opamp current source, rather than the bias voltage itself results in short power on times, as the voltage generated by the biasing circuit is isolated from switching induced perturbations, and the replica bias isolated from the large capacitance (due to decoupling and parasitics) of the original bias voltage which otherwise contributes to a smaller slew rate and large RC time constant. Thus the power on time of the opamp is limited only by the slew rate of the main and replica bias opamps, which can be designed sufficiently large. Since replica biasing can be arranged to increase current source resistance, a large DC gain is also achieved by combining the replica bias technique with a single-stage folded cascode opamp to yield a gain-boosted architecture. A minimum DC gain of 78dB in the first stage was found to restrict finite opamp gain error to less than LSB/4. As such the replica bias approach satisfies two key design criteria for the opamp: a short power on time, and large DC gain. Furthermore, as a large gain is realized with a single stage, simple load compensation and passive common-mode-feedback [9] are afforded, simplifying the design. DC opamp gains for stages 1-2, 3-5, and 6-8 were set at 105dB, 73dB, and 52dB respectively (verified through simulation).

Large signal swings are not required in the replica biasing opamp, thus series current switching is used to modulate the replica biasing opamp's power. Series current switching is used on all tail current transistors without affecting the signal swing at the output of the opamp. Additional switch transistors shown in Figure 4 are used to decrease off time, and avoid floating nodes when the opamp powers off. As the replica bias approach allows for rapid power on times, the Sample and Hold/MDAC opamps are only powered on during hold phases to minimize power, both when CMPS is enabled and disabled.

For rapid power on of the opamps, their bias voltages must be well settled in advance. As bias generating circuits have long power on times, they are powered before the front end sample and hold. The lead time ($t_{bias\text{-}lead}$ in Figure 3, which is digitally programmable) required for bias circuits to settle increases the latency of the pipeline ADC when operating in CMPS mode to 9 clock cycles. Thus the minimum amount of current scaling required for continuous power scaleability is for $f_s$ between 50MS/s and 50/9=5.55MS/s (i.e. only 1:9). Bias circuit power is modulated by series current switches.

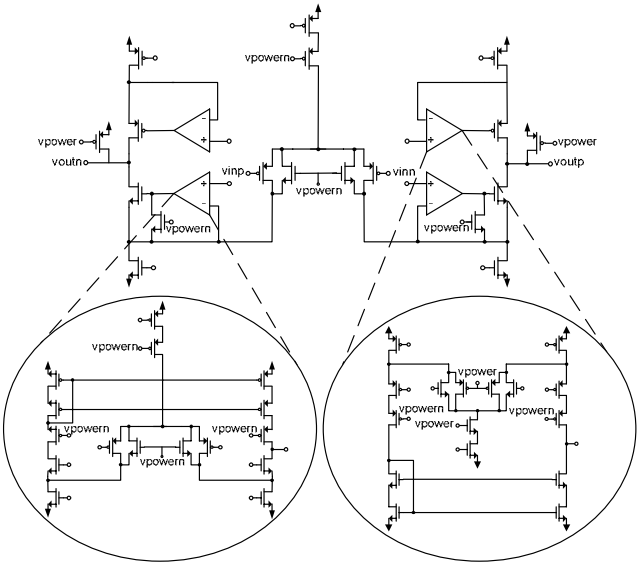


**Figure 6. Rapid power on/off opamp**

## 4.4 Digital state machine:

A digital state machine is used to sequence the active times of each pipeline stage according to Figure 3, where $t_{OFF}$, thus $T_s$, is digitally programmable. The settling time for each stage ($t_{stage}$) is equal to the pulse width of the clock supplied to the state machine ($f_{sm}$). As the state machine consumes power during $t_{OFF}$, it limits the lowest power achievable with CMPS. By reducing $f_{sm}$ however, the state machine power can be reduced. (E.g.) with $f_{sm}$=50MHz, P=570μW, with $f_{sm}$=1MHz , P=11μW. The state machine was conservatively designed to ensure functionality and without synthesis. It is conceivable that if synthesis were used, the state machine power could be further reduced, increasing the power scaleable range.

## 4.5 Non-overlapping clock generator

Non-overlapping clocks required for the MDACs were generated using a commonly used non-overlapping clock generator [7]. The block's power was modulated by passing/blocking the input clock (from an off chip clock generator) via a transmission gate.

## 4.6 Digital error correction

To maximize testability, rather than perform the digital error correction on chip, the digital output from each stage was routed off chip, where a Matlab script was written to emulate the digital error correction on the captured digital output. With the output of each stage available off chip, the functionality of each pipeline stage could be independently and quickly verified. As digital error correction typically consumes less than 5-10% of the total power budget, the exclusion of the block is not significant.

## 5. TESTING AND MEASUREMENTS

A prototype of the power scaleable ADC was fabricated in a 1.8V 0.18µm CMOS process, with 6 metals, MiM Capacitors, and Deep N-Well options, through the Canadian Microelectronic Corporation (CMC). The active area of the prototype was 1.2mm$^2$, and is shown in Figure 7. The chip was packaged in a standard 44 pin CQFP package, and tested with a custom designed 4 layer FR4 dielectric PCB board with a minimum 6mil trace. Sinusoidal inputs were generated using a Rohde & Schwarz SMT03 function generator. An HP 81120A pulse/pattern generator was used to generate the clock to the ADC. The output bits of each pipeline stage were captured using a Tektronix TLA714 logic analyzer, capable of capturing 65,536 points at a time. An Agilent E3620A Dual output DC power supply was used to provide positive and negative voltages to the voltage regulators on the PCB, and off chip reference voltage generators. The measured SNDR and SFDR were deduced from the FFT of the digitized output. To allow for accurate measurement of the ADC core power only, and minimize supply noise, the power pins to the ADC core were not shorted on or off chip with the I/O power pins.

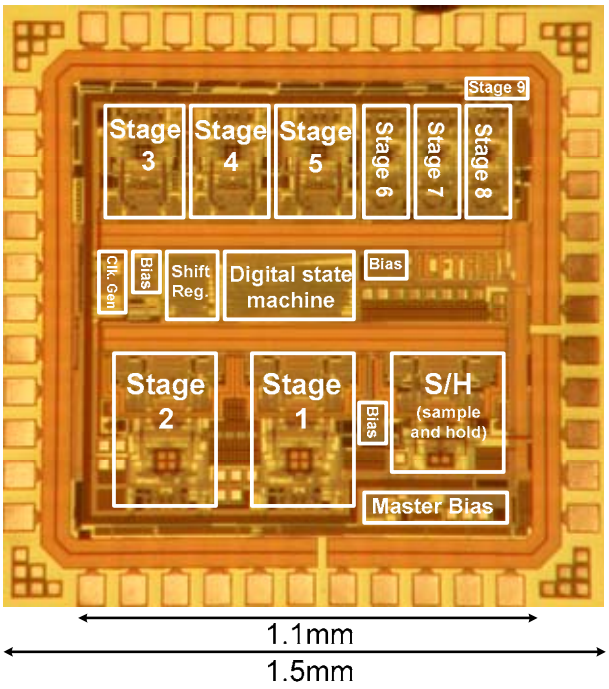


**Figure 7. Fabricated ADC micrograph**

### 5.1 Measured Power, Accuracy results

To demonstrate the multiplying nature of CMPS, bias currents to the ADC were scaled 1:50 and CMPS applied with $f_{sm}$=50MHz, 5.55MHz, and 1MHz, where measured power and SNDR vs. sampling rate are shown in Figure 8. Figure 8 shows CMPS enhances the power scaleable range of current scaling by 50x, where the lowest power for a given $f_{sm}$ is limited by the power of the digital state machine. The ratio of maximum (35mW, 50MS/s) to minimum power (15µW, 1kS/s) achievable when using CMPS with current scaling is ~1:2500. For a given $f_{sm}$ and bias current, SNDR is seen to be virtually constant due to the constant settling times between different sampling rates. This work achieves a larger power scaleable range (1:2500) than [1] (1:1000), and [2] (1:11). Bias currents are scaled by only 1:50 in this work, which is on the order of [2] (1:11), and much less than [1] (1:1000). If the bias currents in this work were further scaled, the power scaleable range would be proportionally larger.

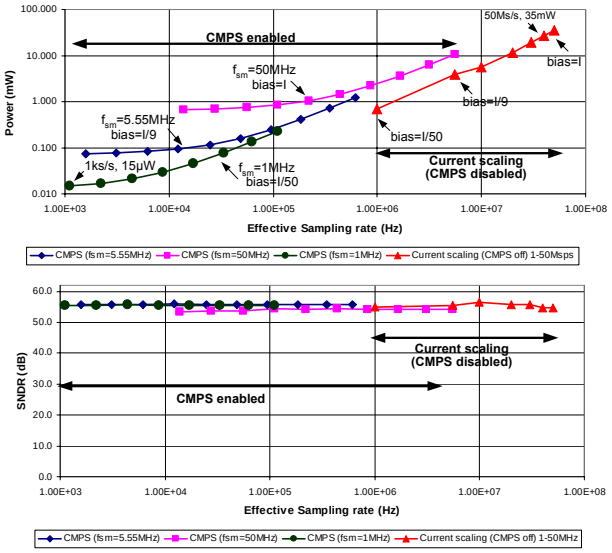


**Figure 8. Power & SNDR vs. $f_s$ for $f_{sm}$=1, 5.55, 50MHz**

Figure 9 shows the performance at the maximum speed of 50MS/s, where an SNDR of 55dB is achieved at $f_{in}$=20.94MHz, and SFDR of 67dB. The INL at $f_s$=50MS/s was +1.06/-1.2, and DNL +0.63/-0.91.

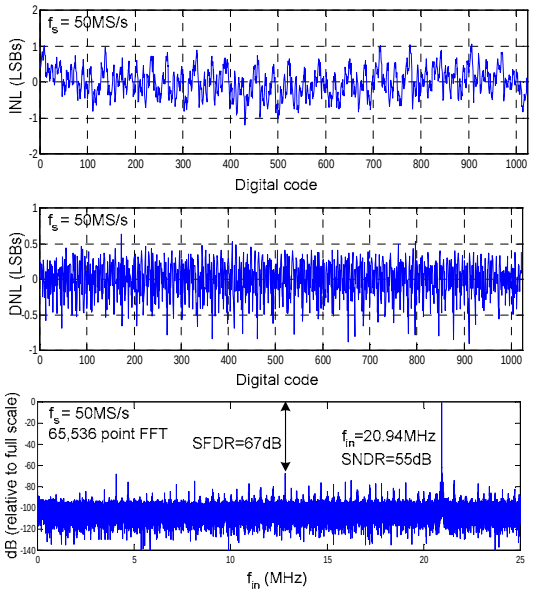


**Figure 9. INL, DNL, FFT of output, $f_s$=50MS/s**

## 5.2 Comparing weak and strong inversion

All bias currents in the ADC were referenced from a single diode-connected master current reference, which via an off-chip resistor set the master on-chip reference current (constant current biasing scheme). A comparison of ADC performance in weak and strong inversion was quantified by reducing the $|V_{GS}|$ of the master current reference for different levels of channel inversion, while measuring the ADC ENOB. The master current source's $|V_{GS}|$ was reduced by 20mV in increments of 2mV from the nominal bias values when the ADC operated at 1Msps and 100ksps using CMPS with $f_{SM}$=50MHz (strong inversion, no current scaling), and when the ADC operated at 1Msps and 100ksps in nominal pipeline mode with scaled bias currents (weak inversion). To ensure $V_{GS}$ variations affected settling time, the nominal bias voltage (i.e. without any $V_{GS}$ reduction) of the master current source in each case was such that 7-8 effective bits were measured (i.e. ADC was bandwidth limited) for the different sampling rates before $|V_{GS}|$ was decreased. Figure 10 shows the reduction of ADC ENOB versus $|V_{GS}|$ offset applied. The results verify that extended variations in bias current to scale power with sampling rate result in increased sensitivity of the ADC to bias voltage variations, which can be caused by transistor threshold mismatch, or parasitically coupled noise. Hence it may be inferred from the results that as the ADC is operated deeper in weak inversion, the poorer yield will be. The bias sensitivity results allow one to infer yield trends without resorting to the time and resource consuming task of individually measuring variations in ADC accuracy for hundreds of different chips. Since the CMPS architecture is able to retain strong inversion biasing for lower sampling rates, it shows more robustness to small node voltage fluctuations.

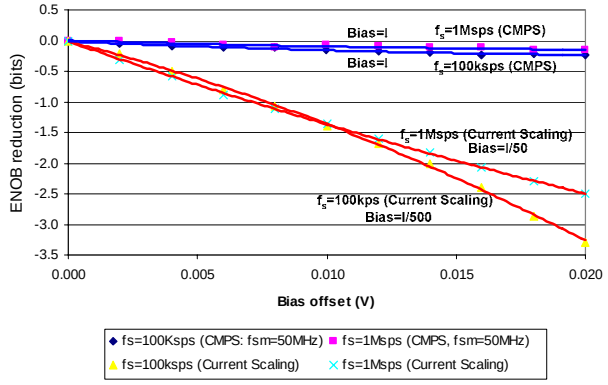


**Figure 10. ENOB sensitivity to offset**

## 6. CONCLUSIONS

A power scaleable pipelined ADC was presented, which achieves power scalability without requiring extensive current scaling, thus is more robust than previous solutions. The keys to power scalability at high sampling rates were the use of a current modulation based architecture, and the development of a novel rapid power on opamp, which by virtue of a replica bias technique, is able to completely and quickly power on/off. Measured results from a prototype fabricated in 0.18µm CMOS show the combination of CMPS and current scaling over a much smaller range (1:50) compared to previous works results in an ADC which had its power a function of sampling rate between 1kS/s (15µW), and 50MS/s (35mW) while maintaining an SNDR of 54-56dB over the entire power scaleable range. A comparison of bias voltage sensitivity using CMPS and current scaling was performed, where the robustness of the CMPS architecture was verified.

## 7. ACKNOWLEDGEMENTS

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