IMRAN AHMED

CAREER GOAL/ EXPERTISE

- To enable and deliver both at the technical and business level, next generation mixed-signal technologies using state-of-the-art 'smart-analog' design approaches.

EDUCATION

2004-2008 **PhD, Electrical Engineering**

University of Toronto

- Thesis: "Pipelined ADC enhancement techniques"
  - Developed and prototyped (0.18um CMOS) calibration technique to cancel DAC nonlinearity due to capacitor mismatch + low DC opamp gain errors in a very short amount of time with a low complexity digital solution
  - Developed and prototyped (0.18um CMOS) architecture to remove front-end sample and hold in pipeline ADC which has no skew related matching requirements in the layout
  - Developed and prototyped (0.18um CMOS) novel pipelined ADC architecture which does not require any opamps, thus saving large amounts of power
  - 3.94/4.00 GPA in PhD courses

2002-2004 **MASc, Electrical Engineering**

University of Toronto

- Developed and prototyped (0.18um CMOS) novel pipeline ADC architecture with a power consumption that scaled with operating speed from 1kS/s (15uW) to 50MS/s (35mW)
- 4.00/4.00 GPA in MASc courses, A+ in thesis

1997-2002 **BASc, Engineering Science, Electrical option**

University of Toronto

- Had ranked #1 in electrical option, and overall top 10 in program in numerous terms
- Final year average > 90% , graduated with 'Honor standing'
- Engineering Science considered as the premier undergraduate Engineering program in Canada

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RELAVENT WORK EXPERIENCE

2008-present **Senior Mixed Signal IC Designer**

Kapik Integration, Toronto

- Developed cutting edge circuits for RF and mixed signal applications
- Architectural development using digitally enhanced techniques to enable significantly improved performance over prior architectures

2007 **Student-Intern**

Broadcom, Bunnik, Netherlands

- 3-month student internship
- Investigated novel low power pipelined ADC architectures

2000-2001, 2002, 2004 **Student-intern/IC design engineer**

Snowbush Microelectronics, Toronto

- 16 month student internship from 2000-2001, and consulting role in 2002, 2004
- Worked on physical design of several cutting edge designs (e.g.: high speed CDR, 8-bit 200MS/s ADC, 10-bit 150MS/s ADC
- Worked on analog/digital design of high speed CDR, high speed ADC
- Developed Verilog/VHDL models for digital flow

2002 - present **Teaching Assistant**

University of Toronto

- Served as a teaching assistant in many 2nd and 3rd year electronics courses
- Have TA'd tutorials, lab sessions, and occasionally lectured

RELAVENT AWARDS

- 2008 Analog Devices 'Outstanding Student Designer Award'
- 'Young Scientist Award' for best student paper at ESSCIRC 2007
- 1st place and Best-Overall submission in 2005 DAC/ISSCC student design contest
- In 2006 Received prestigious 'Canada Graduate Scholarship' from National Sciences and Engineering Research Council (NSERC); total value $70,000
- In 2002 Received prestigious 'Post Graduate Scholarship' from National Sciences and Engineering Research Council (NSERC); total value $34,000
- Ontario Graduate Scholarship 2002, 2004-2006
- University of Toronto Fellowship 2002-present

KEY PUBLICATIONS

Journal Papers:

- I. Ahmed, and D.A. Johns, "An 11-bit 45MS/s pipelined ADC with rapid calibration of DAC errors in a multi-bit pipeline stage", *Journal of Solid State Circuits (JSSC)*, vol 43, pp.1626-1637, July 2008

- I. Ahmed, and D.A. Johns, "A high bandwidth power scaleable sub-sampling 10-bit pipelined ADC with embedded sample and hold", *Journal of Solid State Circuits (JSSC),* vol 43, pp.1626-1637, July 2008

- I. Ahmed, and D. A. Johns, "A 50MS/s (35mW) to 1kS/s (15uW) power scaleable 10b pipeline ADC using rapid power-on opamps and minimal bias current variation", *Journal of Solid State Circuits (JSSC),* vol 40, pp. 2446-2455, Dec. 2005

Conference papers:

- I. Ahmed, J. Mulder, and D. Johns, "A 50MS/s 9.9mW Pipelined ADC with 58dB SNDR in 0.18um CMOS Using Capacitive Charge-Pumps", *To appear in IEEE International Solid State Circuits Conference (ISSCC),* Feb. 2009*,* San Francisco, USA

- I. Ahmed, and D.A. Johns, "An 11-bit 45MS/s pipelined ADC with rapid calibration of DAC errors in a multi-bit pipeline stage", *IEEE European Solid State Circuits Conference (ESSCIRC)*, September 2007, Munich, Germany

- I. Ahmed, and D.A. Johns, "A high bandwidth power scaleable sub-sampling 10-bit pipelined ADC with embedded sample and hold", *IEEE European Solid State Circuits Conference (ESSCIRC)*, September 2007, Munich, Germany

- I. Ahmed, and D.A. Johns, "DAC nonlinearity and residue gain error correction in a pipelined ADC using a split-ADC architecture", *IEEE PRIME conference,* June 2006*,* Otranto, Italy

- I. Ahmed, and D.A. Johns, "A 50MS/s (35mW) to 1kS/s (15uW) power scaleable 10b pipeline ADC with minimal bias current variation", *IEEE International Solid State Circuits Conference (ISSCC),* February 2005*,* San Francisco, USA

VOLUNTEER /EXTRA-CURRICULAR INVOLVEMENT

- Active volunteer in IEEE
  - In charge of organizing/leading large volunteer effort to aid in the administration/audio-visual support for the International Solid State Circuits Conference (ISSCC)
  - In charge of maintaining/updating ISSCC main website
  - Have volunteered in >500 hours since 2004 to help with ISSCC
- Have been active in various campus organizations (e.g.) MSA, anti-racism office

INTERESTS

Traveling, fitness, photography, composing music