A 50MS/s (35mW) to 1kS/s (15 μW) Power Scaleable 10b pipelined ADC with minimal bias current scaling

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Motivations

Applications:

• Systems which have reconfigurable bandwidth, compliancy with multiple standards, and/or operation at multiple operating rates require flexible circuit blocks which have a power that reduces with operating speed

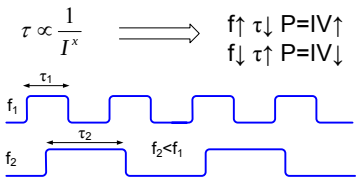
Industrial design:

• A single ADC design can be targeted for use in multiple applications which have different requirements with respect to power and speed, saving design and implementation time and costs of designing several individually power optimized ADCs

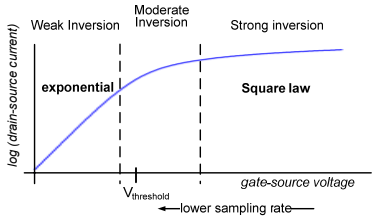
State of the art

• ADC dominated by analog power (static), which does not scale with sampling rate explicitly (contrasted with digital circuits which do scale according to fCV^2)

• Analog settling time is a function of bias current supplied, thus reducing bias currents as sampling rate reduced scales power with sampling rate



• For large reductions in sampling rate thus bias currents, analog blocks biased in active mode shift from strong inversion to Weak Inversion (WI) operation



• In WI drain-source current (I_{DS}) is a more sensitive function of gate-source voltage (V_{GS}), as a result in weak inversion small perturbations of V_{GS} from nominal values due to (e.g.)

- transistor threshold mismatch
- noise coupled to V_{GS}

causes large variations of I_{DS}

• Thus in WI, ADC will suffer from poorer yield, and be less robust, which is highly undesirable in industrial applications

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Abstract

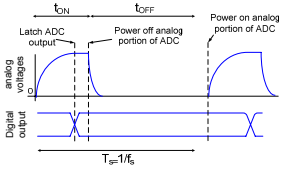
A new opamp with a short power on time, and a current modulation technique, are used to implement a 10b 1.5b/stage pipelined ADC (fabricated in 0.18μm CMOS) which has a scaleable power between 1kS/s (15μW) to 50MS/s (35mW), while only varying the bias currents by a factor of 50. An SNDR of 54-56dB was measured for all sampling rates.

Approach of this work

• Motivated by desire to minimize bias current scaling

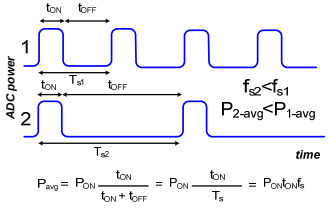
• Approach works by powering off static power blocks (analog) between output conversions:

• Once analog portion of ADC reaches desired settling accuracy, digital outputs are latched, and the analog portion of the ADC powered off until another analog input to the ADC is to be sampled as shown below



• This Current Modulated Power Scale (CMPS) approach works by keeping a fixed t_{ON} (analog power on time, which uses a fixed bias current) and varying the time the ADC is powered off (t_{OFF})

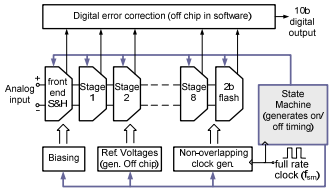
• Different power and sampling rates are realized by only varying the time the ADC is off, where time averaging yields a power that scales with sampling rate as shown below



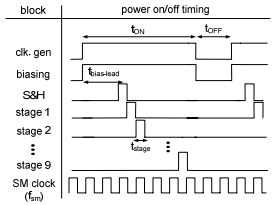
$$P_{avg} = P_{ON}\frac{t_{ON}}{t_{ON}+t_{OFF}} = P_{ON}\frac{t_{ON}}{T_s} = P_{ON}t_{ON}f_s$$

• When used *with* current scaling, CMPS multiples the power scaleable range of current scaling, since for any current scaled sampling rate, the ADC can be powered off between conversions yielding a further reduction in ADC power without further reduction in bias currents

• In this work CMPS was applied to a 10b 1.5b/stage pipeline architecture as shown below



• Architecture is identical to a conventional pipeline ADC, except for the addition of a state machine (SM), which is used to power on/off the blocks in the ADC according to CMPS as shown below



• When CMPS is enabled, $f_{s\text{-}max}$ is (latency of ADC)$^{-1}$ which is lower than max f_s attainable with a pipeline architecture, which is (stage delay)$^{-1}$

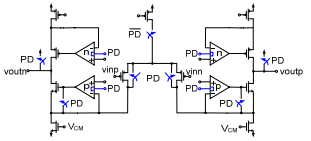
• To achieve power scalability for all sampling rates afforded by the pipeline architecture there are two modes of operation:

1.) *CMPS enabled:* used to achieve power scalability up to (latency)$^{-1}$ (=5.55MS/s)

2.) *CMPS disabled, ADC operated as a conventional pipeline ADC* (i.e. without powering off stages between conversions): and current scaling used to achieve power scalability for sampling rates not allowable with CMPS, i.e. (latency)$^{-1}$ → (stage delay)$^{-1}$ (= 5.55MS/s → 50 MS/s in this work)

• Need rapid power-on opamp to achieve high sampling rates with CMPS (key challenge), as such a novel rapid power-on opamp was developed for this work

• Architecture is a variant of a folded cascode gain-boosted approach, where differences are highlighted in blue



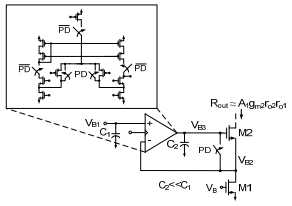
• Usually opamps are powered on/off by grounding their bias voltages during the off time, which has a slow power-on time because:

- bias voltages have high capacitances to reduce noise, and are set by small currents
- large capacitance, small current setting bias node results in long slew time to reach steady state, thus so too the opamp they bias

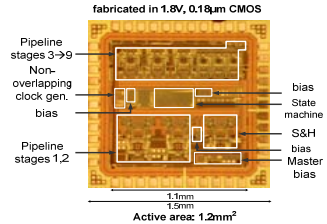
• In the opamps of this work a copy of the bias voltage is switched via a replica biasing approach as shown below, resulting in rapid power-on as copied bias has lower capacitance and driven by a larger current

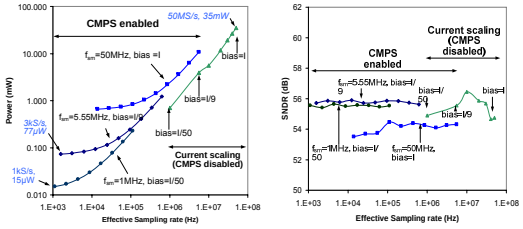
• Combination of replica bias with cascode current source increases current source output impedance, allowing for a large DC opamp gain using only a single stage. Single stage allows:

- load compensation
- a simple passive CMFB



Measured results

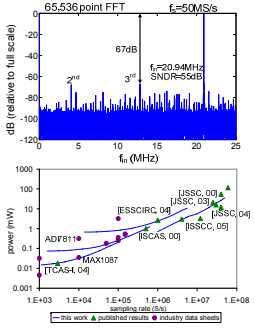


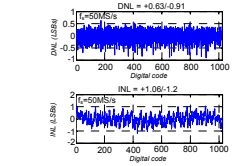


• CMPS multiples power scaleable range of current scaling by 50x

• Minimum power is given by state machine, the power of which is reduced by reducing its clock (e.g. shown above for f_{sm}=50MHz, 5.55MHz, 1MHz)

• Only need 1:9 variation in bias currents for continuous power scale, but also show 1:50 to show effectiveness of CMPS in achieving very low power





Technology	1.8V, 0.18um CMOS
Resolution	10 bit
Full scale input	1.6V p-p
Area	1.2mm²
f_s (power) range	1kS/s (15μW) - 50MS/s (35mW)
bias current scaling	1:50
Performance at 50MS/s	
Power	35mW
SNDR (fin=20.94MHz)	55dB (8.8b ENOB)
SFDR (fin=20.94MHz)	67dB
DNL/INL	0.63/-0.91, 1.06/-1.2

Summary

• Very large power scaleable range using current modulated approach which enhances power scaleable range of current scaling

• Use of current modulation at high speeds attained by use of novel rapid power-on opamp

• ADC power is amongst the best published and industry ADCs over entire variation of f_s, showing this work to be highly effective for ADC power scaling

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