PRIME 2006
Session 3A3.02

DAC nonlinearity and residue gain error correction in a pipelined ADC using a split-ADC architecture

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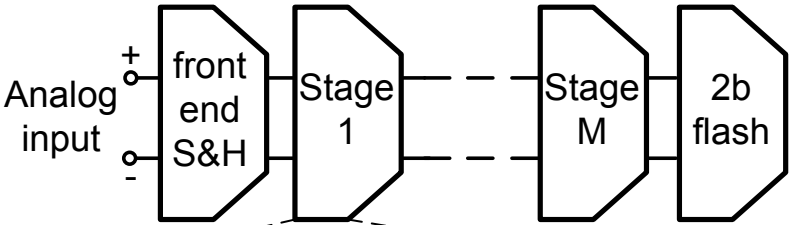
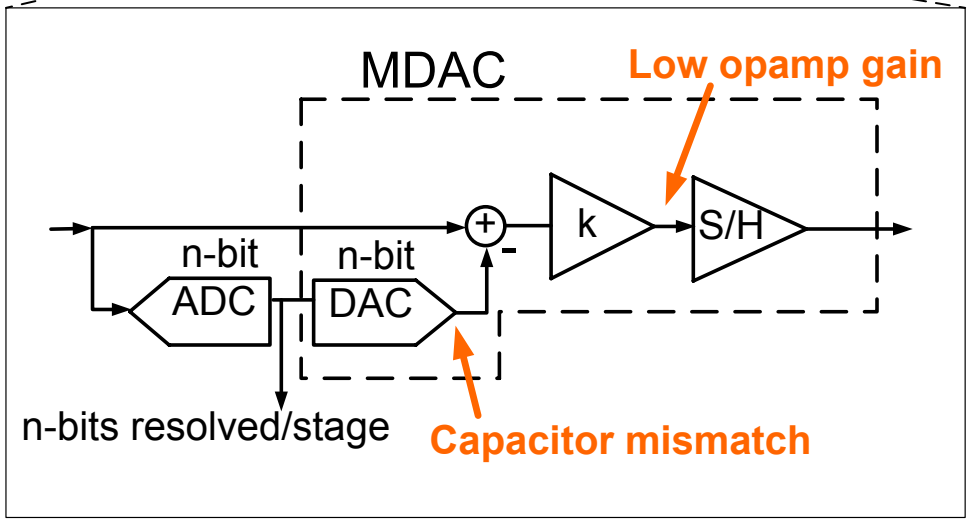
Overview

- Goals + Motivations of work
- State of the art
- Approach of this work
- Simulation results in Simulink and Spice
- Summary

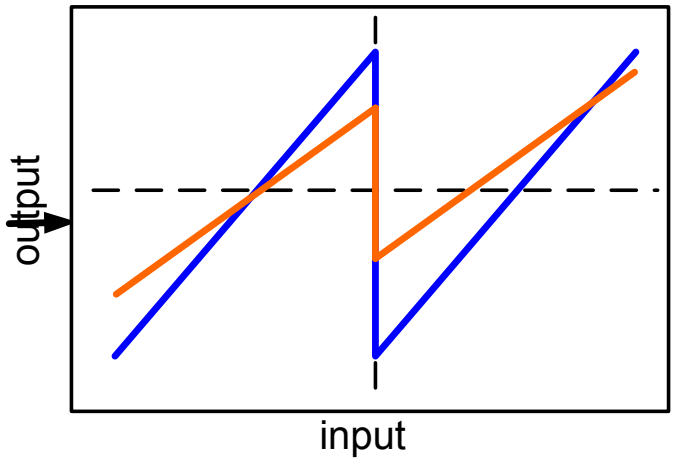
Goals + Motivations

- **Digitally** calibrate in **background** following nonidealities:
  - **1.)** Low opamp gain
  - **2.)** Capacitor mismatch
- Achieve fast calibration
  - Saves testing time





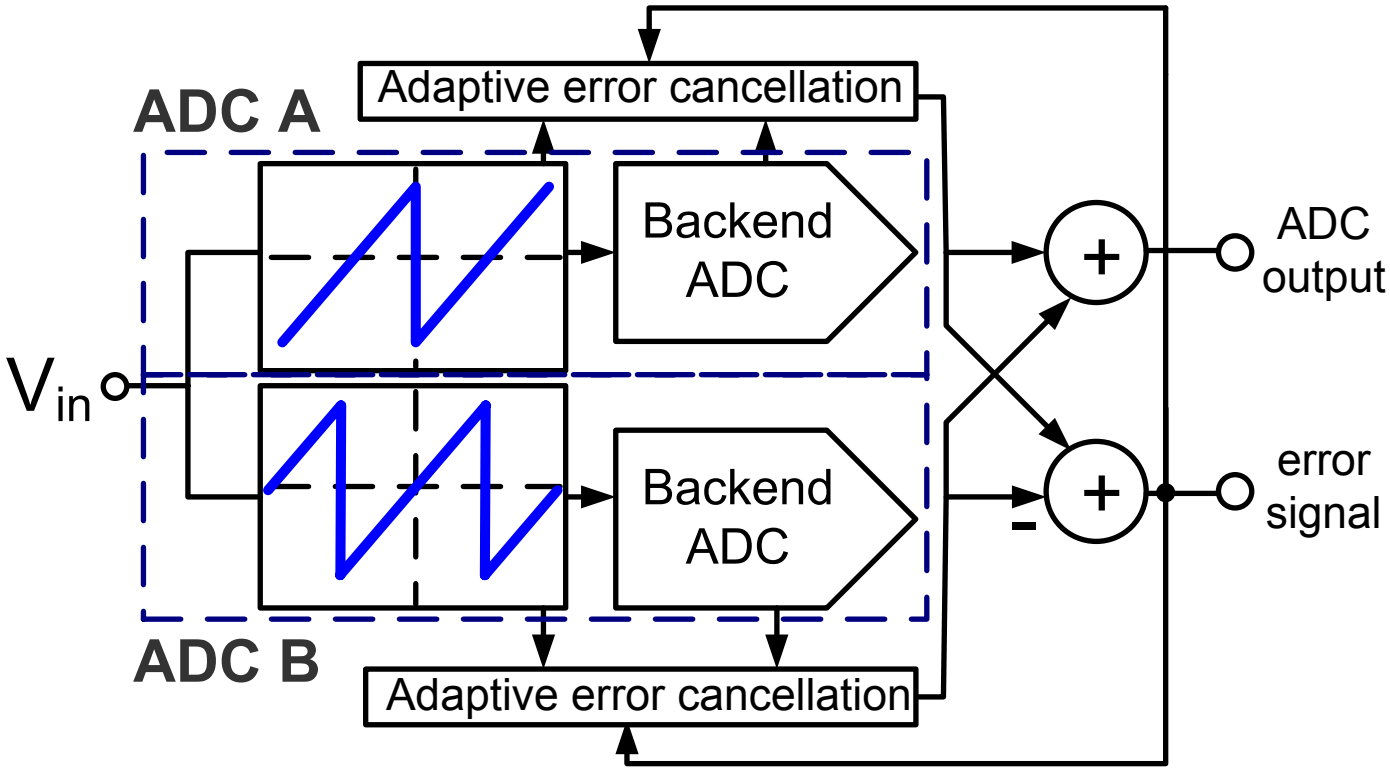
Example 1-bit residue transfer characteristic



Prior works

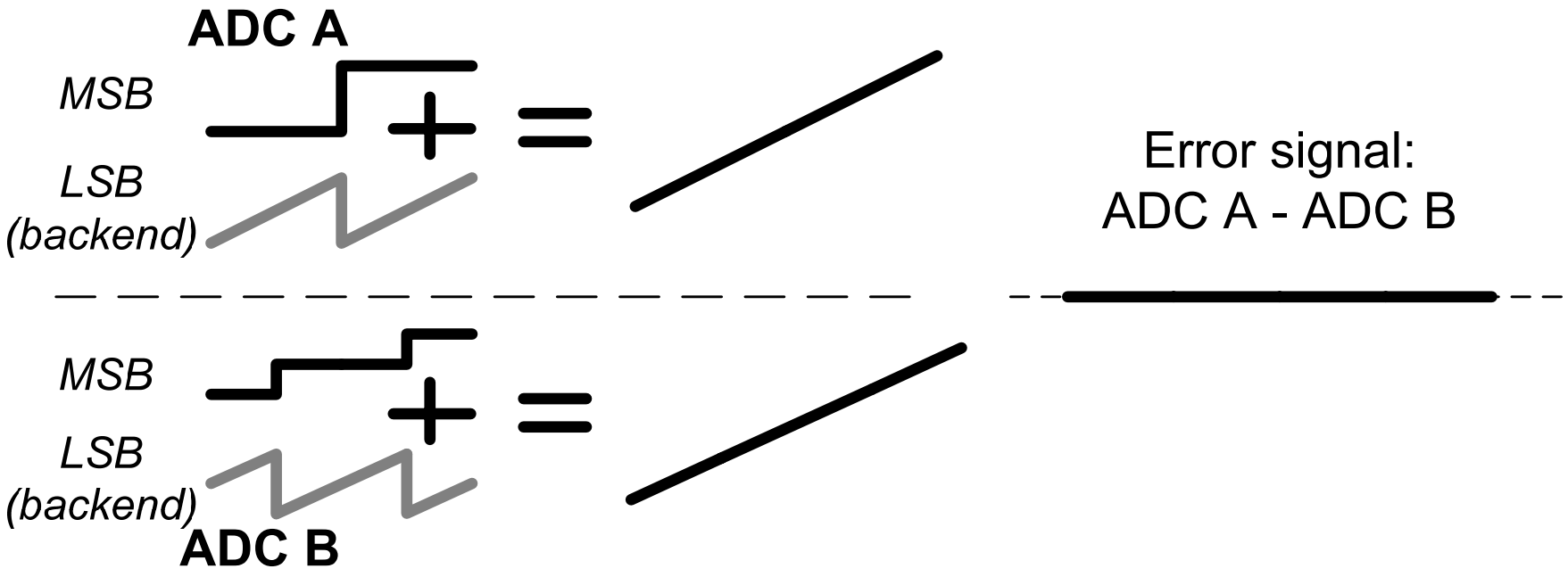
- Background w/digital calibration
  - Use statistical techniques to estimate errors → long time
  - E.g.: [I. Galton TCAS-II March 2000] $2^{25} = 3x10^7$ clock cycles to calibrate for 14b linearity
  - Generally need ~2^{2N} (N=resolution in bits) clock cycles for calibration with statistical approaches
- New architecture: Split ADC [J. Li, U.K Moon, TCAS-II, Sept 2003], [McNeill et al, ISSCC 2005]
  - Corrects opamp gain error in very short time
- We use split ADC in this work to also correct for DAC errors

Split ADC overview



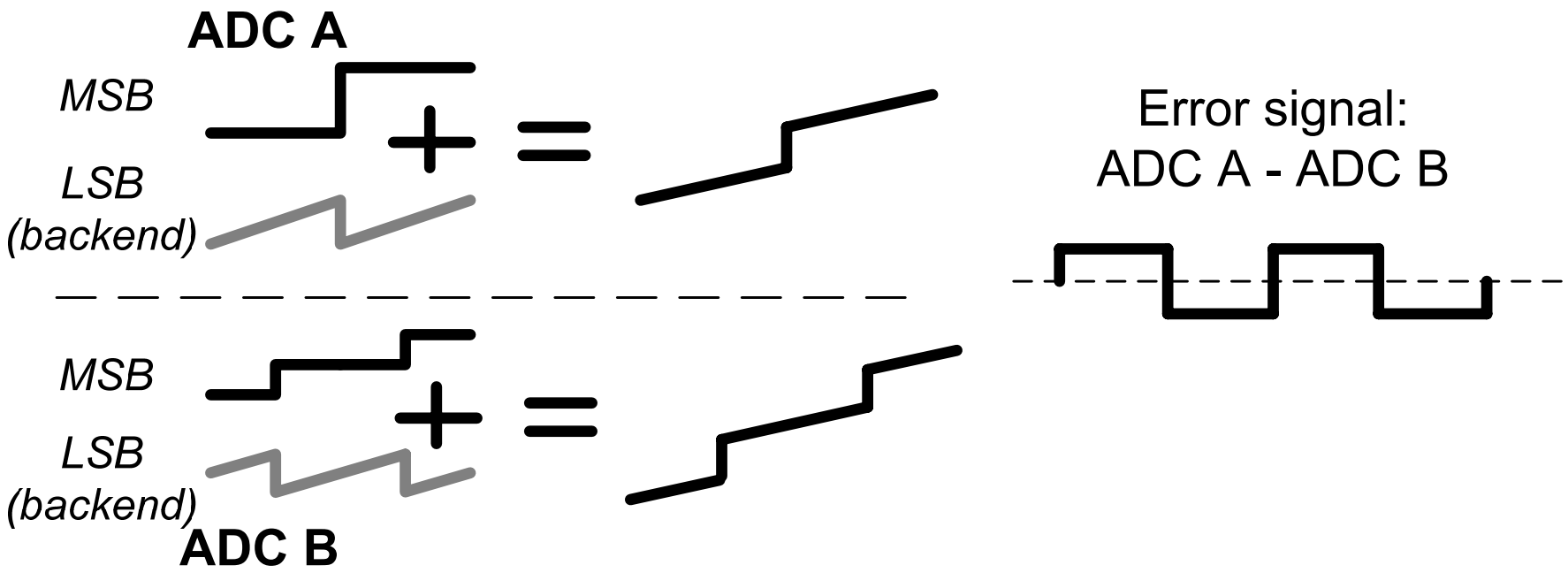
- Two ADCs have different paths to the same output due to redundancy in residue transfer characteristic
- Difference of ADCs used for calibration, sum is ADC output
- **Each ADC ½ resolution, ½ area, thus ½ power of overall ADC**

Split ADC example - ideal



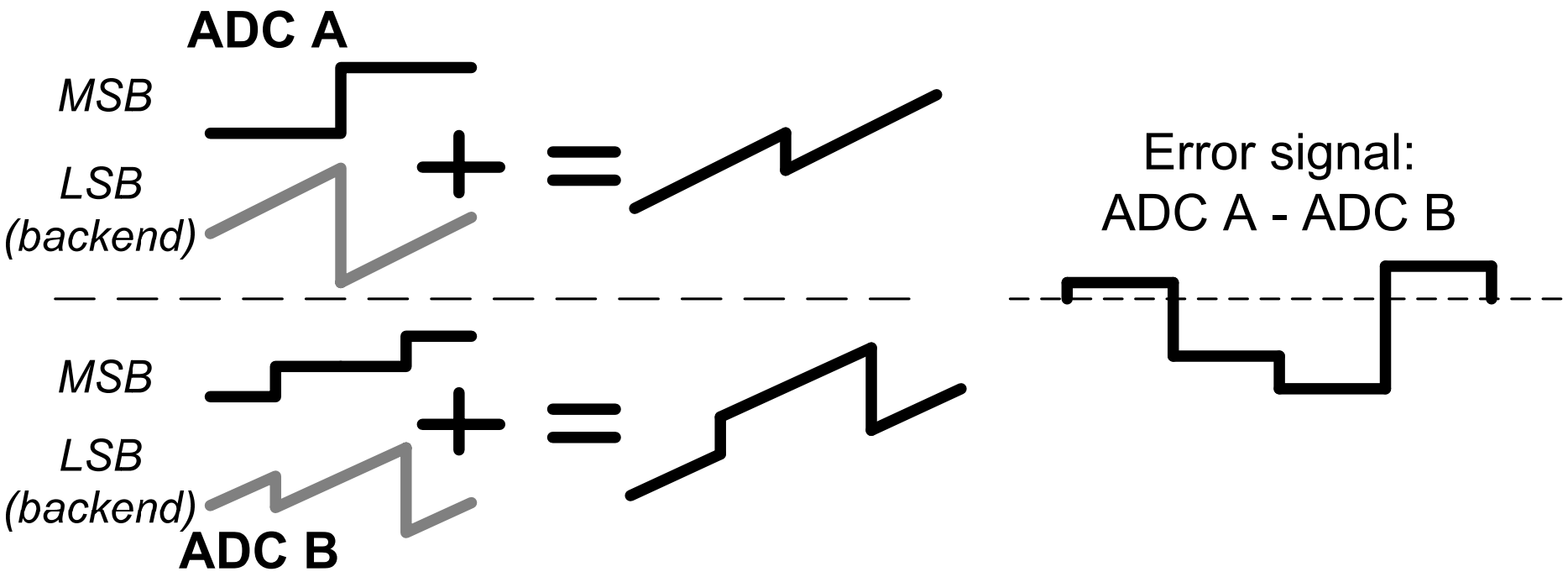
- With no errors difference in ADC A,B is zero
  (only 1b MSB shown to simplify illustration)

Split ADC example – w/gain error



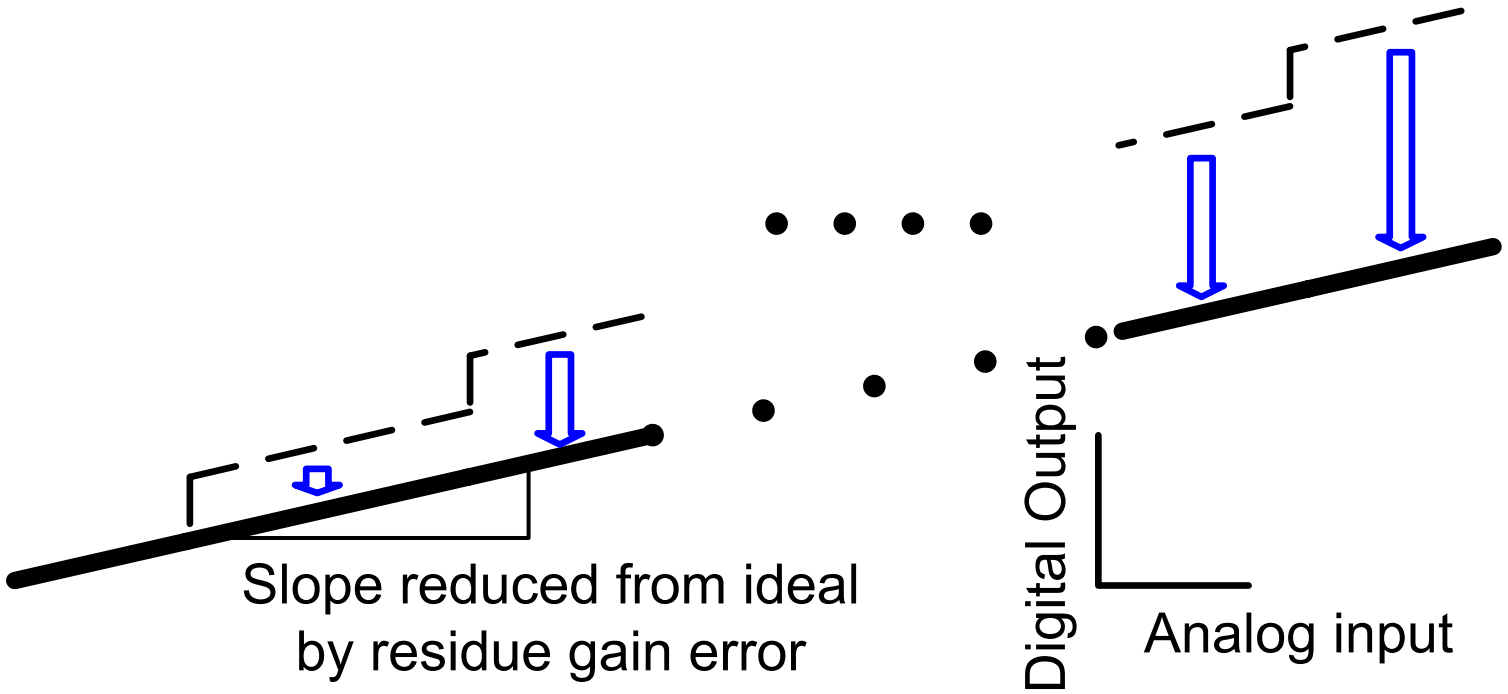
- Because of different paths in each split ADC
  → ADC A, B different outputs with gain errors
- Prior split ADC works corrected only gain errors

Split ADC example – w/DAC error



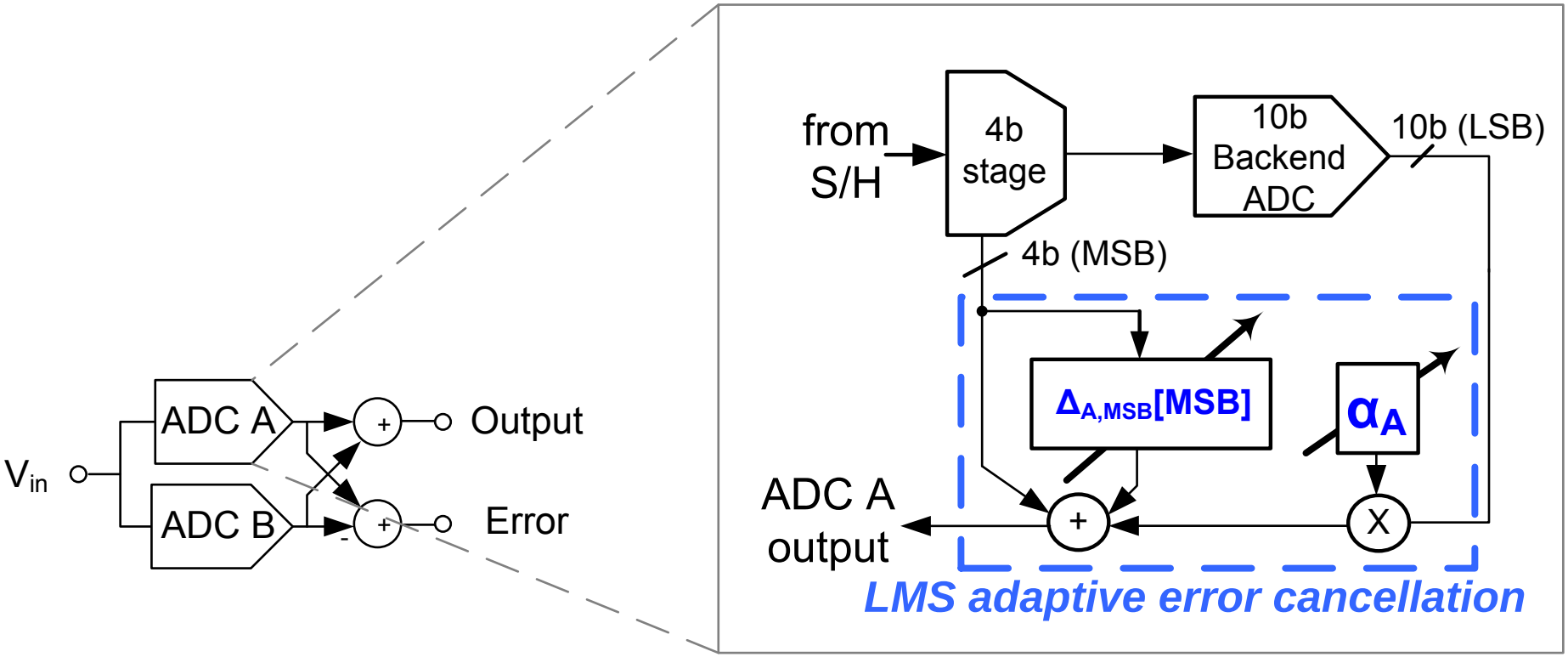
- ADC A, B different outputs also when DAC errors present
- In this work in addition to gain error also correct for DAC error in multi-bit pipeline ADCs

Correcting DAC and gain error



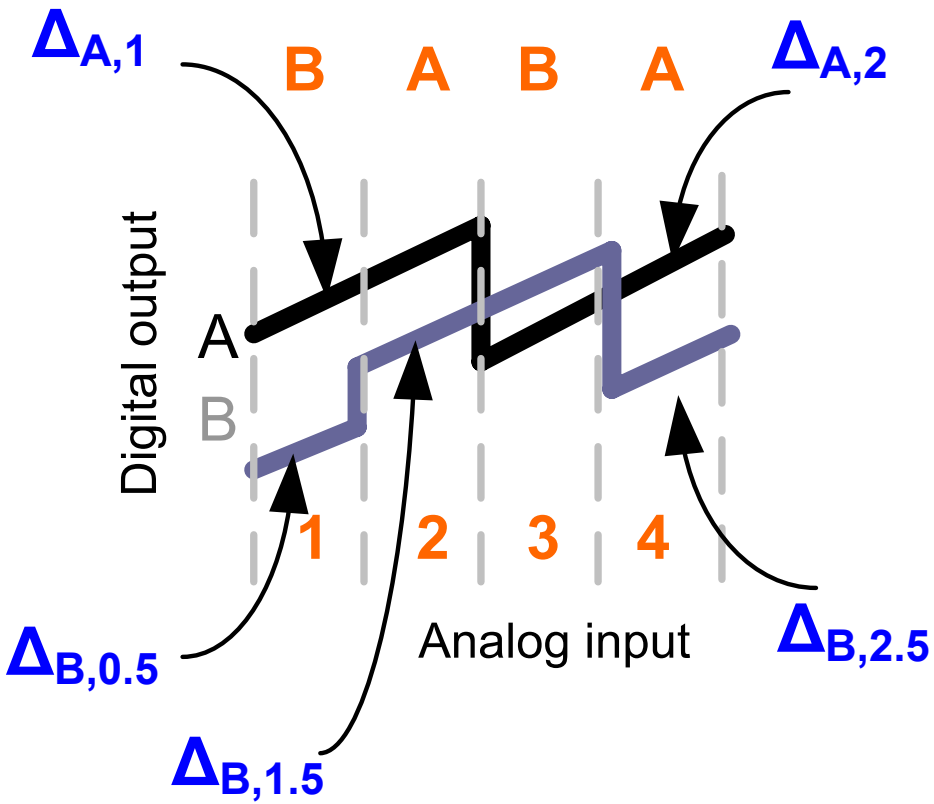
- Shift segments of digital code to fall along straight line
- Each shift is different (function of MSB) so DAC error is also corrected

Architecture



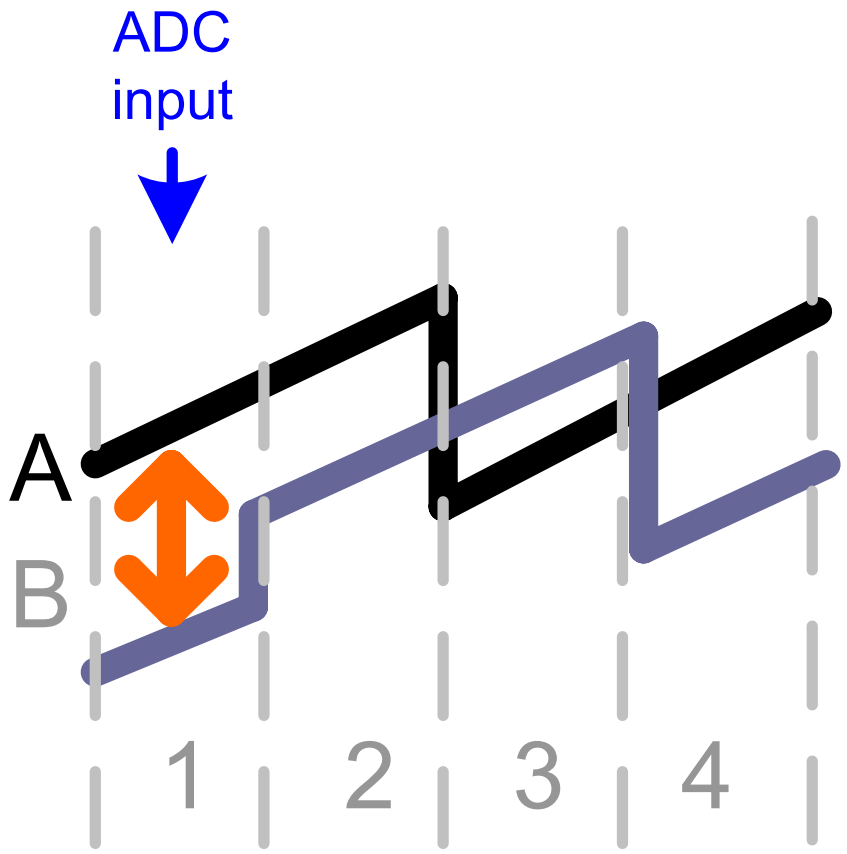
- $\Delta_{i,MSB}$ corrects gain, DAC errors
- α_i term corrects mismatch between split ADCs
- Calibration requires reasonably “busy” for calibration

Calibration algorithm



- Shift everything on the right by equal amounts
- Alternately keep parameters of ADCs A,B constant in regions 1,2,3,4

Calibration example



- Shift everything on the right by equal amounts

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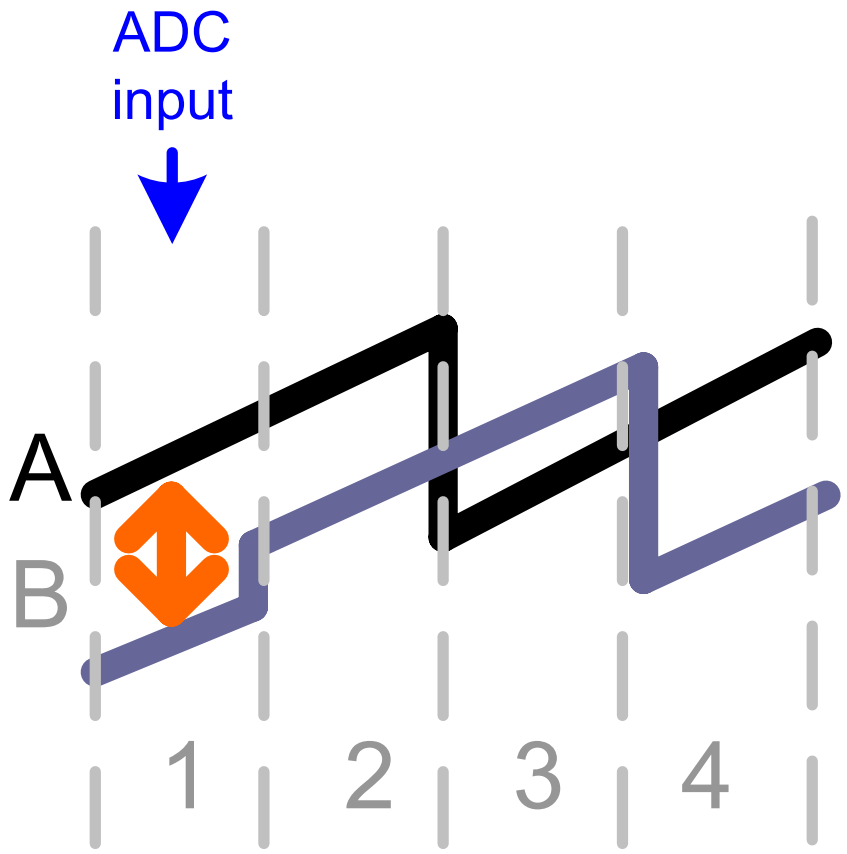
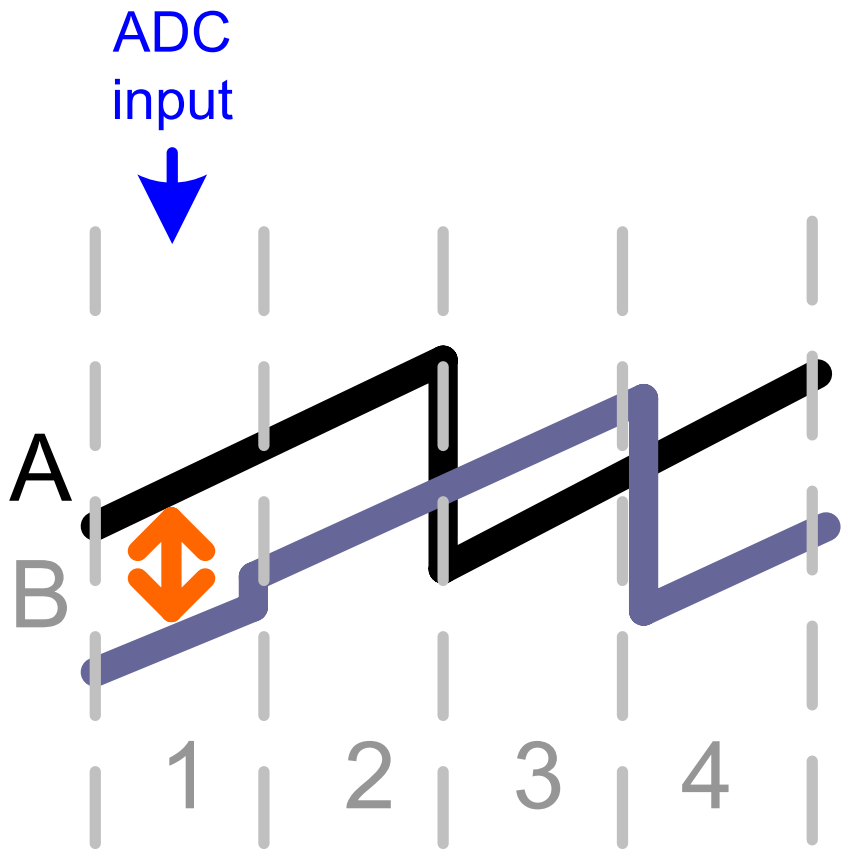


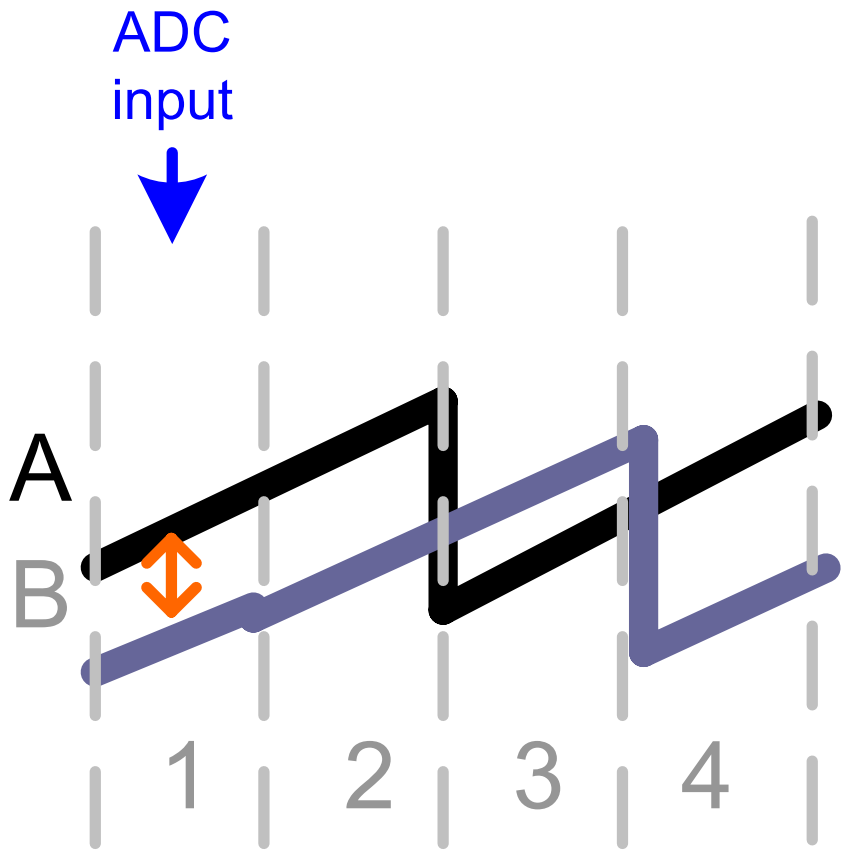
- $\Delta_{A,1} -= k$, $\Delta_{A,2} -= k$, $\Delta_{B,1.5} -= k$, $\Delta_{B,2.5} -= k$

Calibration example



- $\Delta_{A,1} = k$, $\Delta_{A,2} = k$, $\Delta_{B,1.5} = k$, $\Delta_{B,2.5} = k$

Calibration example



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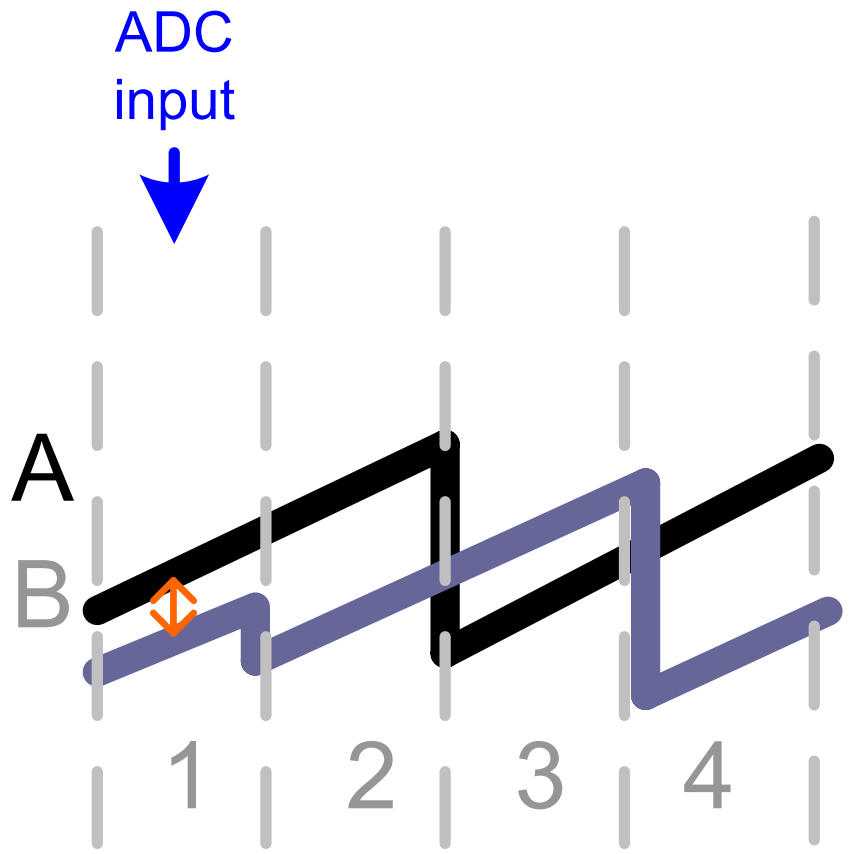

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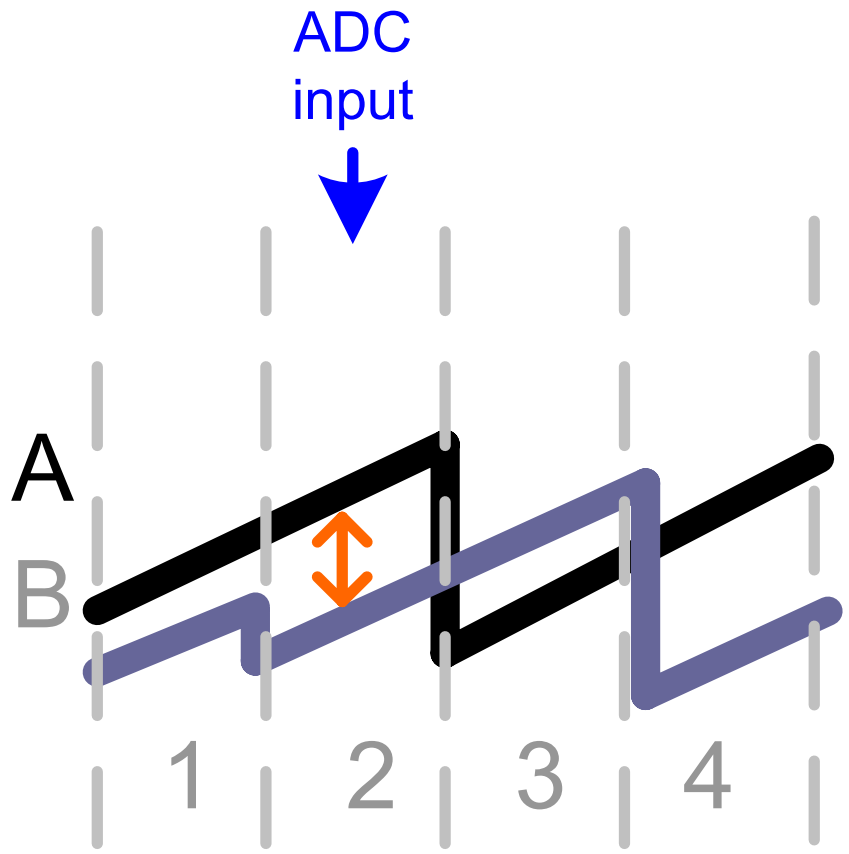
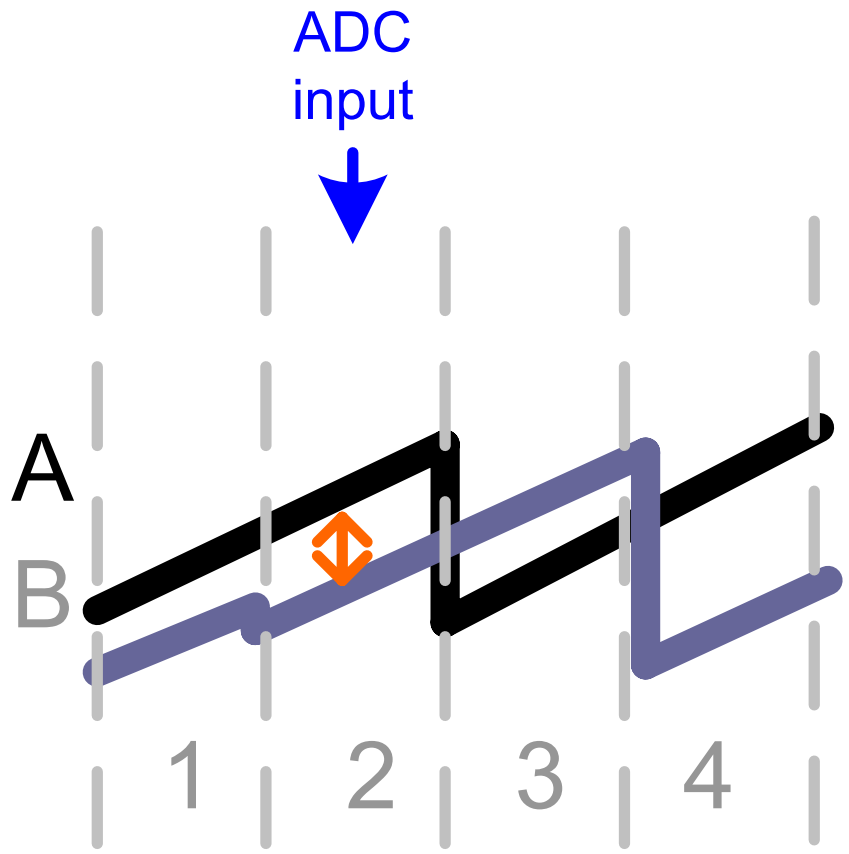


- $\Delta_{A,2}$+= k, $\Delta_{B,1.5}$+= k, $\Delta_{B,2.5}$+= k

Calibration example



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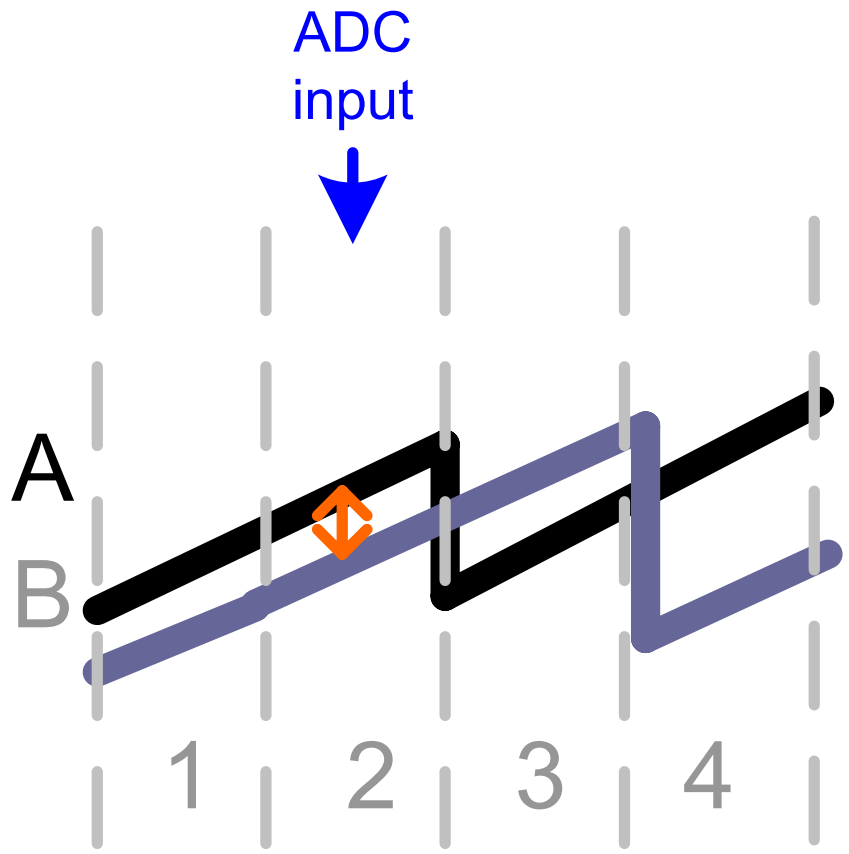
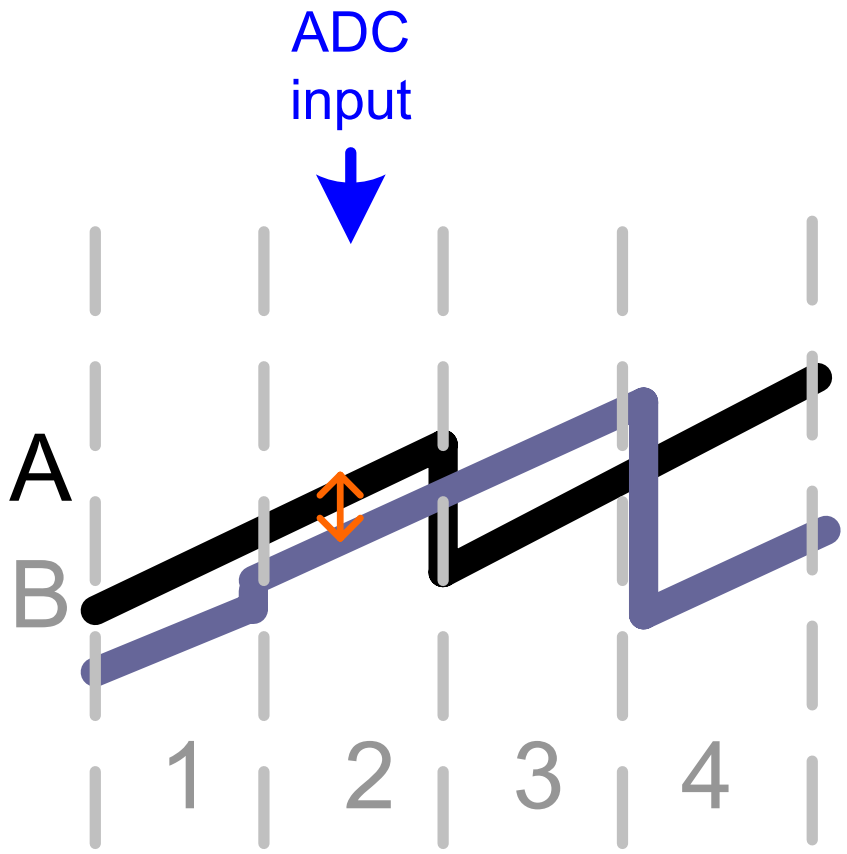
Calibration example



- $\Delta_{A,2} \mathrel{+}= k$, $\Delta_{B,1.5} \mathrel{+}= k$, $\Delta_{B,2.5} \mathrel{+}= k$

Calibration example



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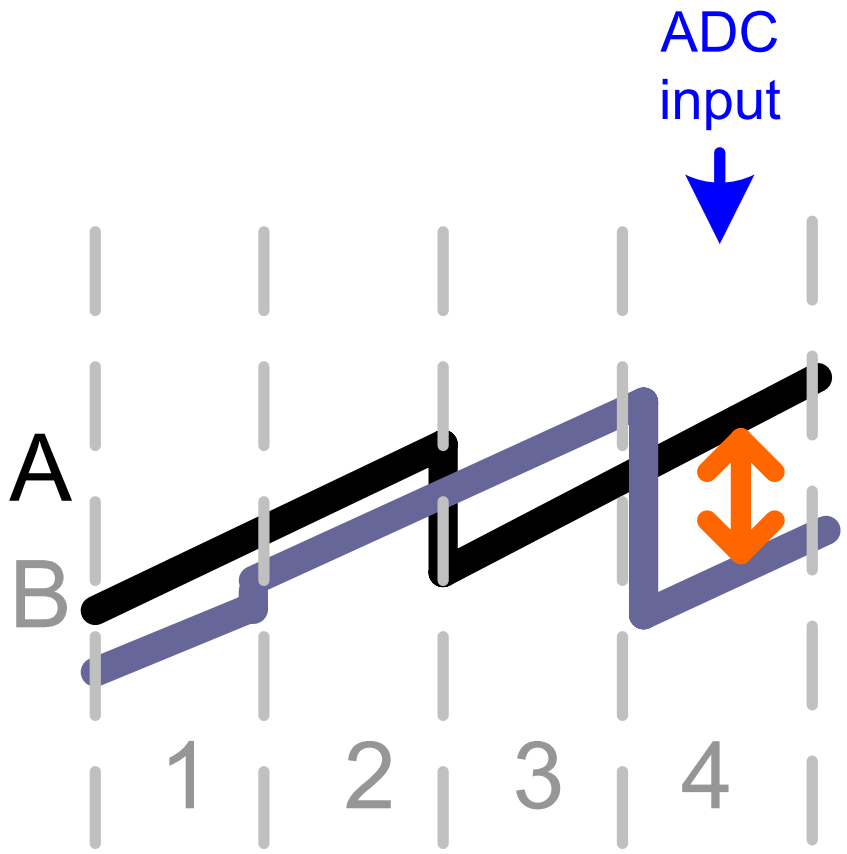
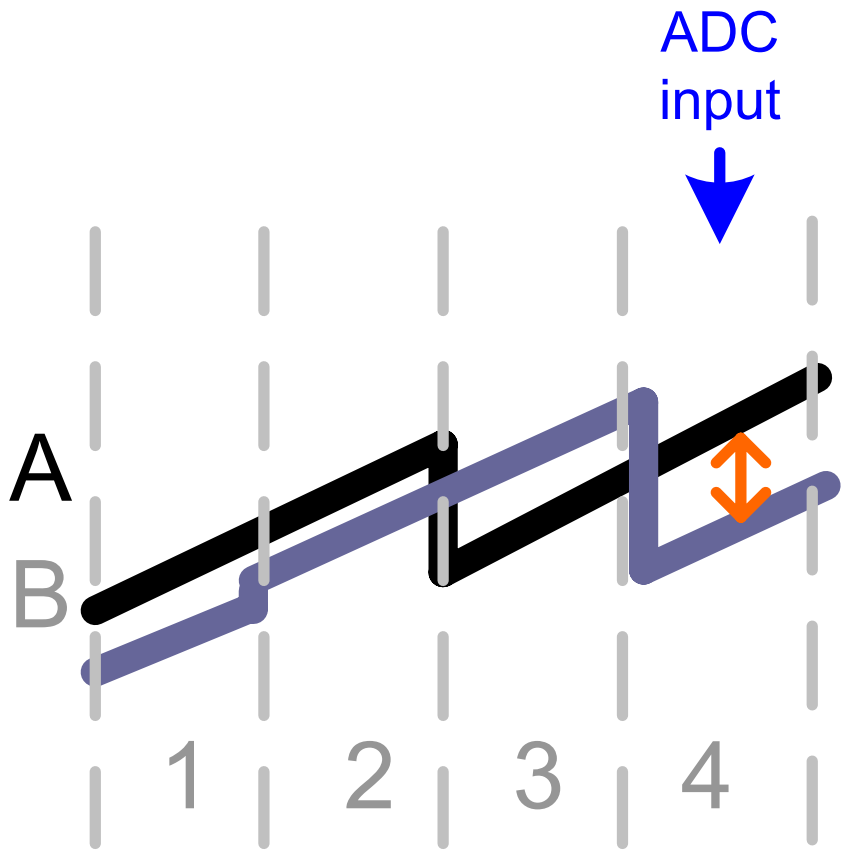
Calibration example



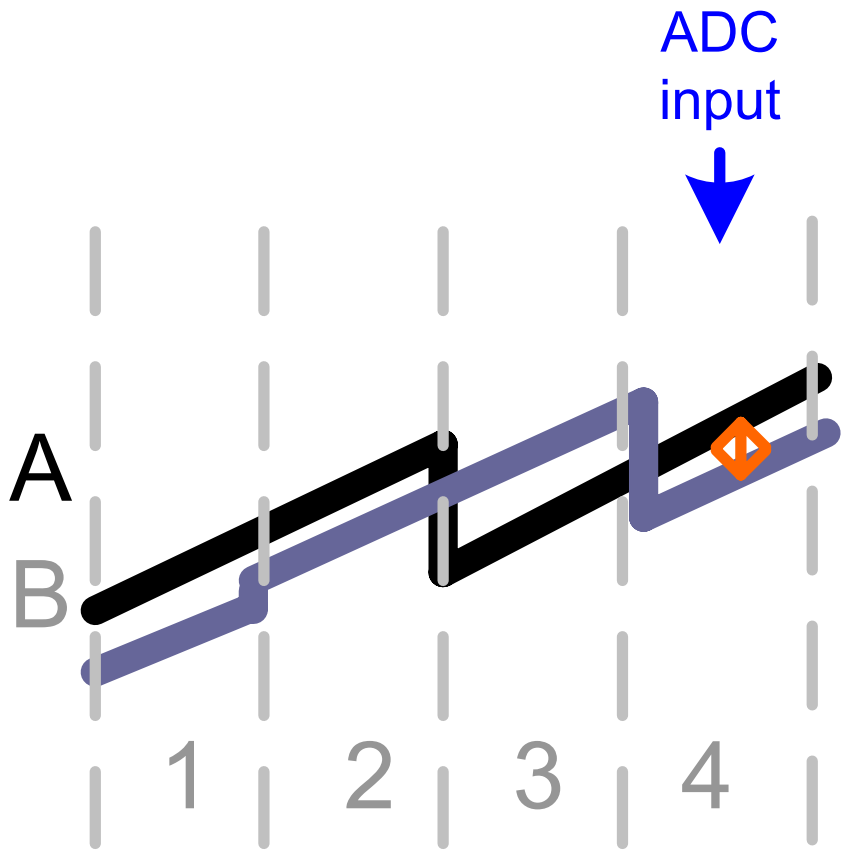
- $\Delta_{B,2.5} \mathrel{+}= k$

Calibration example



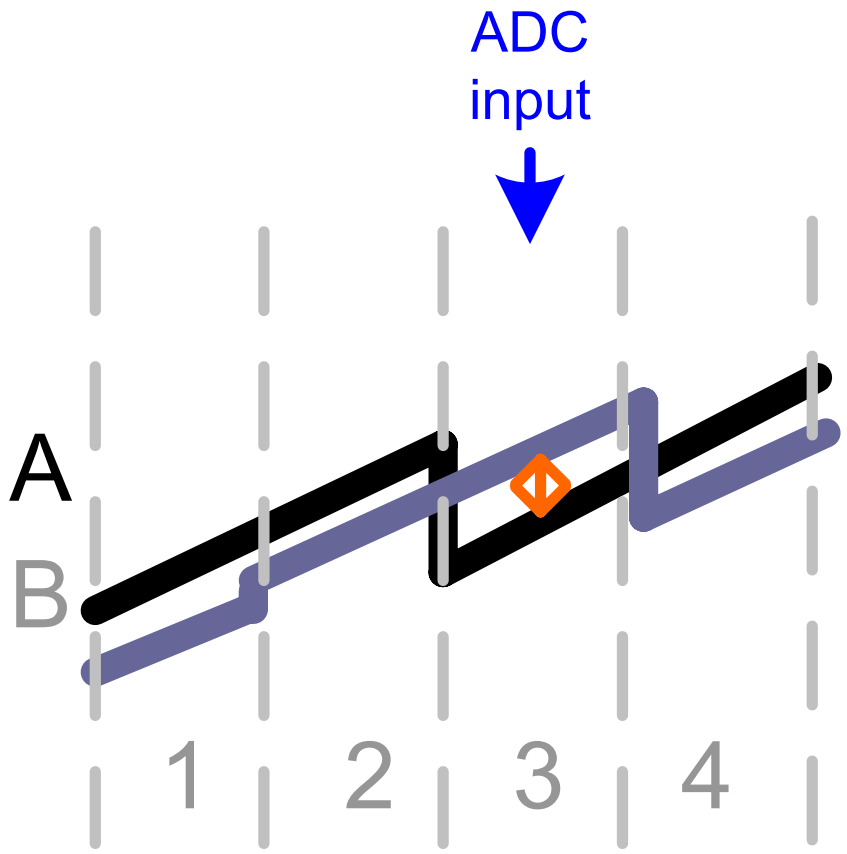
- $\Delta_{B,2.5}$+= k

Calibration example



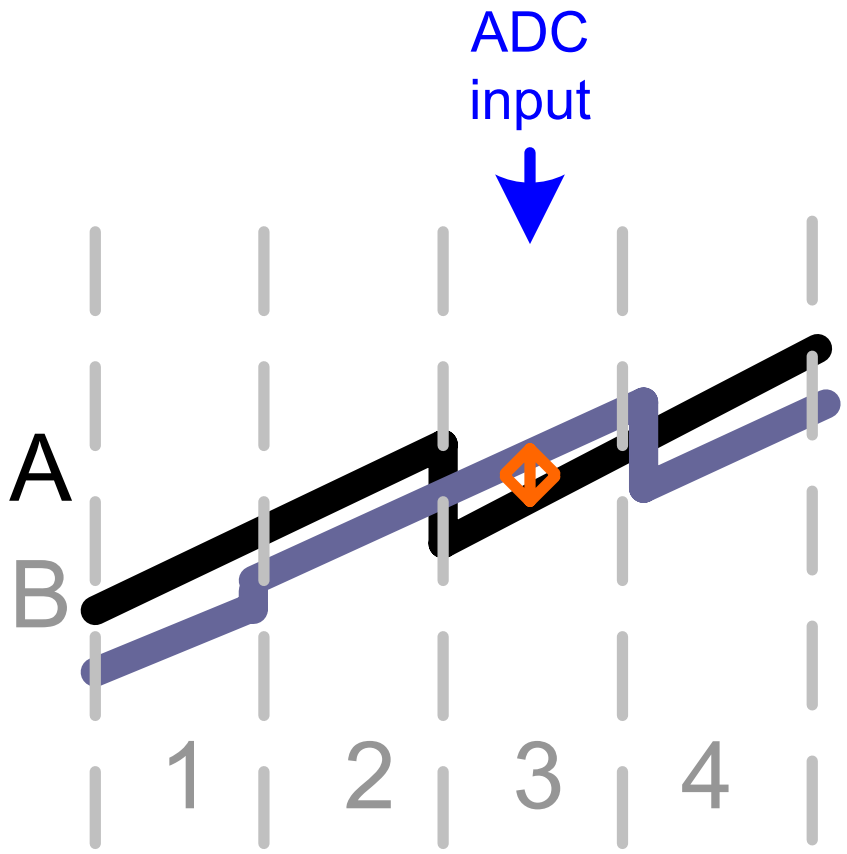
- $\Delta_{\mathbf{B,2.5}} \mathrel{+}= k$

Calibration example



- $\Delta_{A,2} \mathrel{+}= k$, $\Delta_{B,2.5} \mathrel{+}= k$

Calibration example



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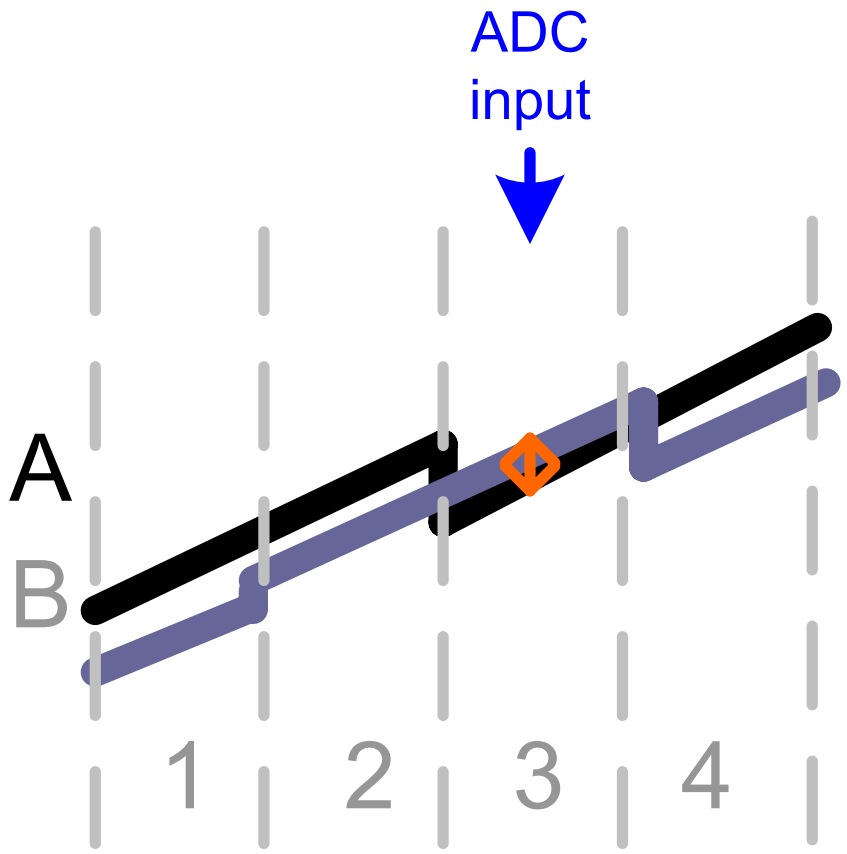

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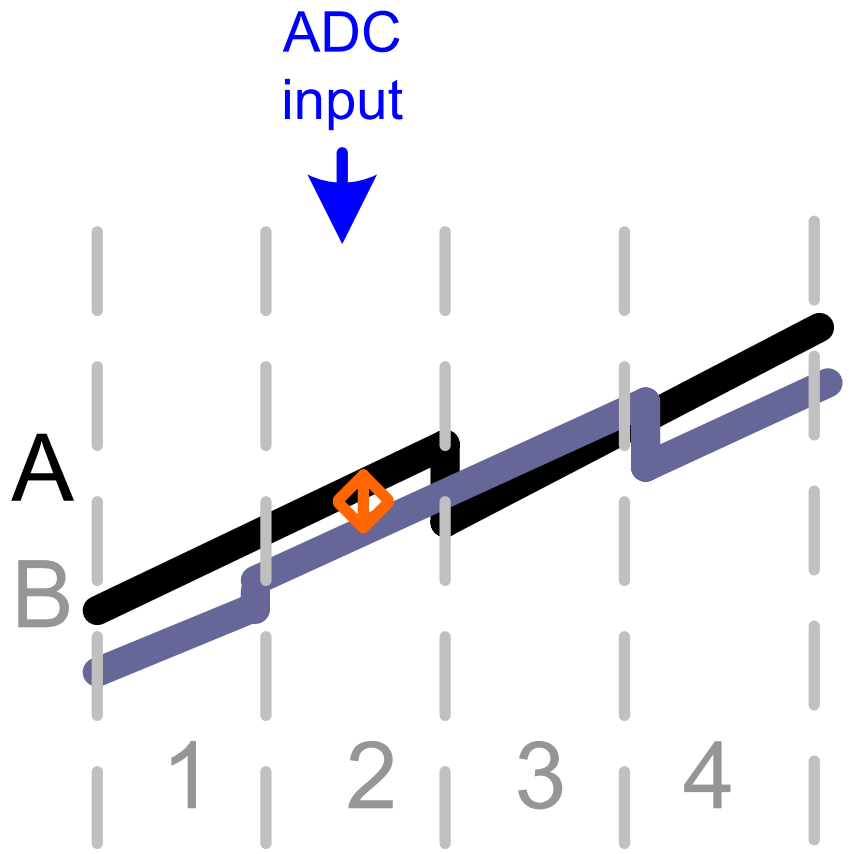
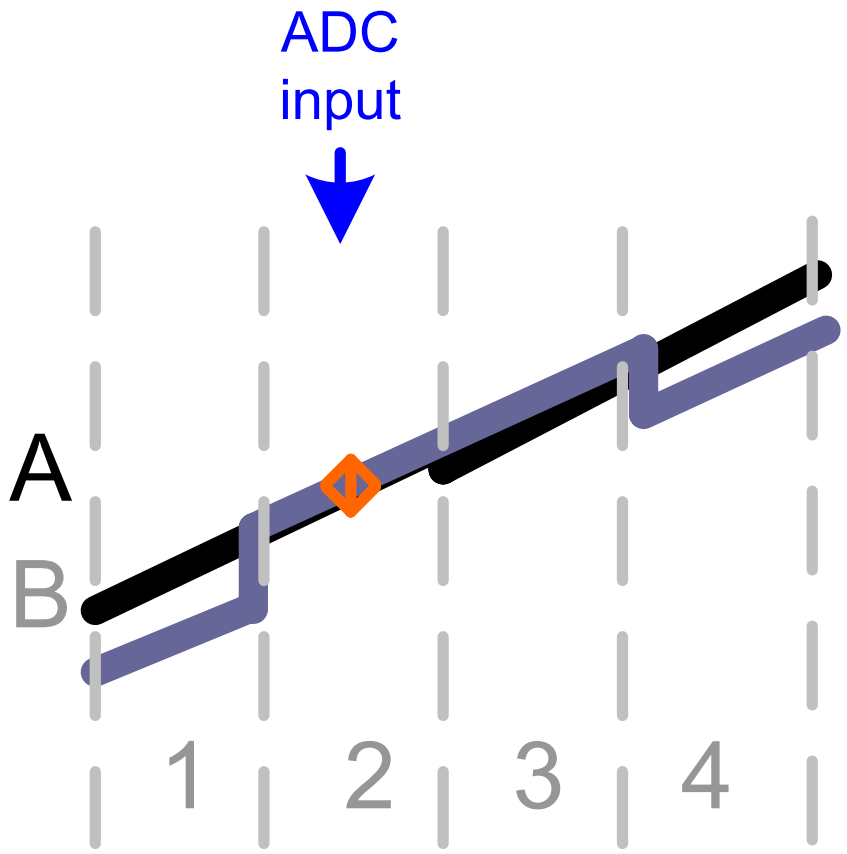


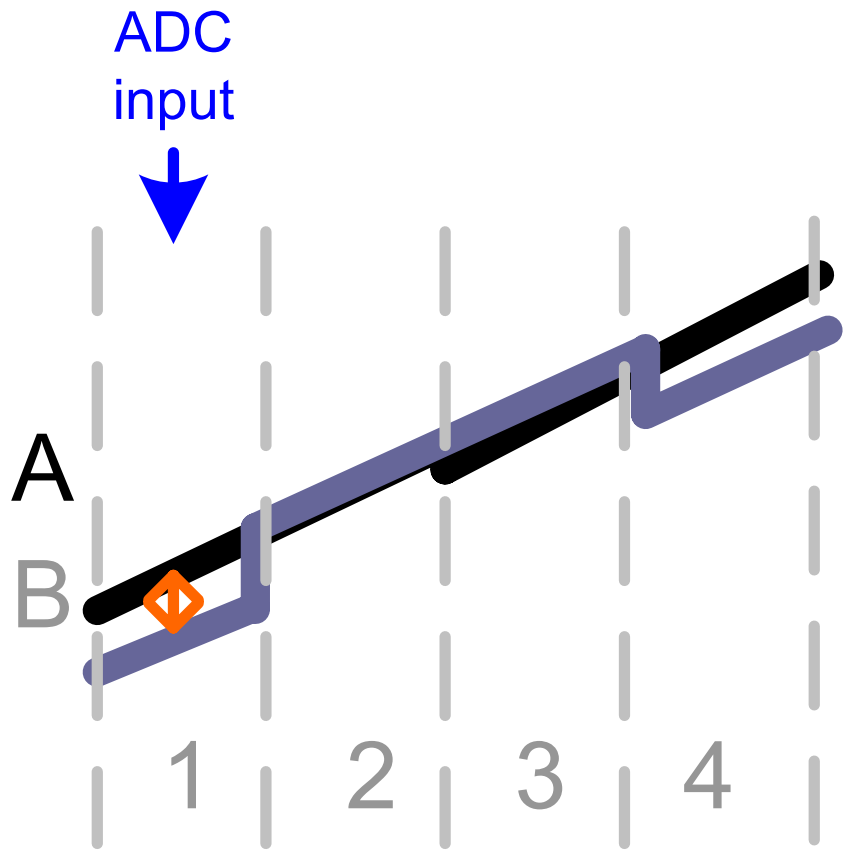
- $\Delta_{A,2} \mathrel{+}= k$, $\Delta_{B,1.5} \mathrel{+}= k$, $\Delta_{B,2.5} \mathrel{+}= k$

Calibration example



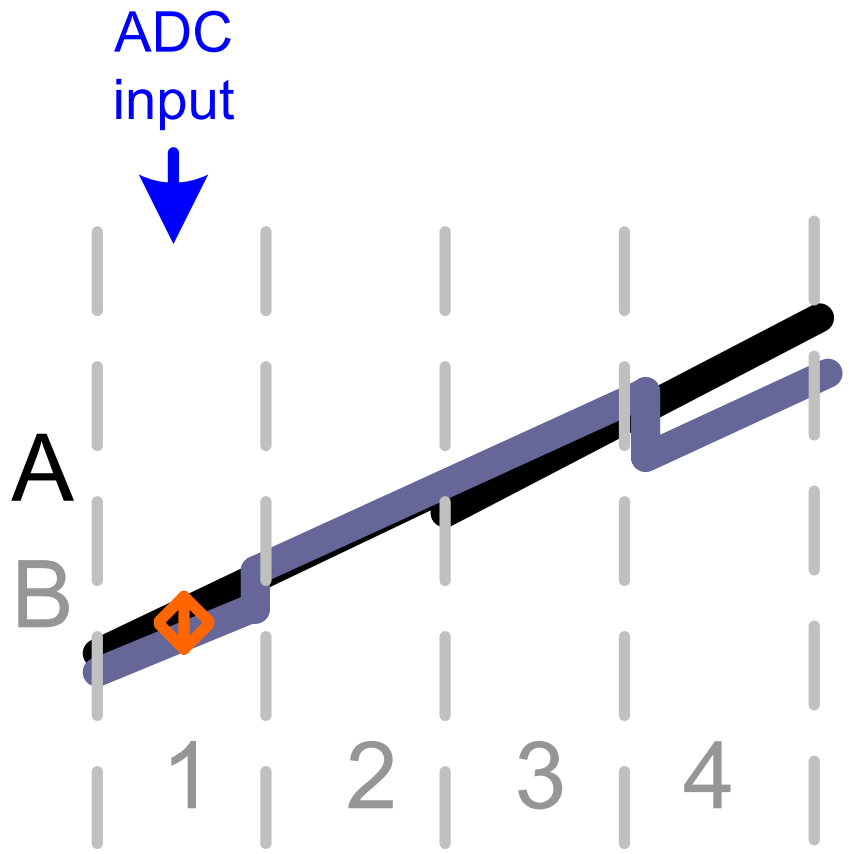
- $\Delta_{A,2} = k$, $\Delta_{B,1.5} = k$, $\Delta_{B,2.5} = k$

Calibration example



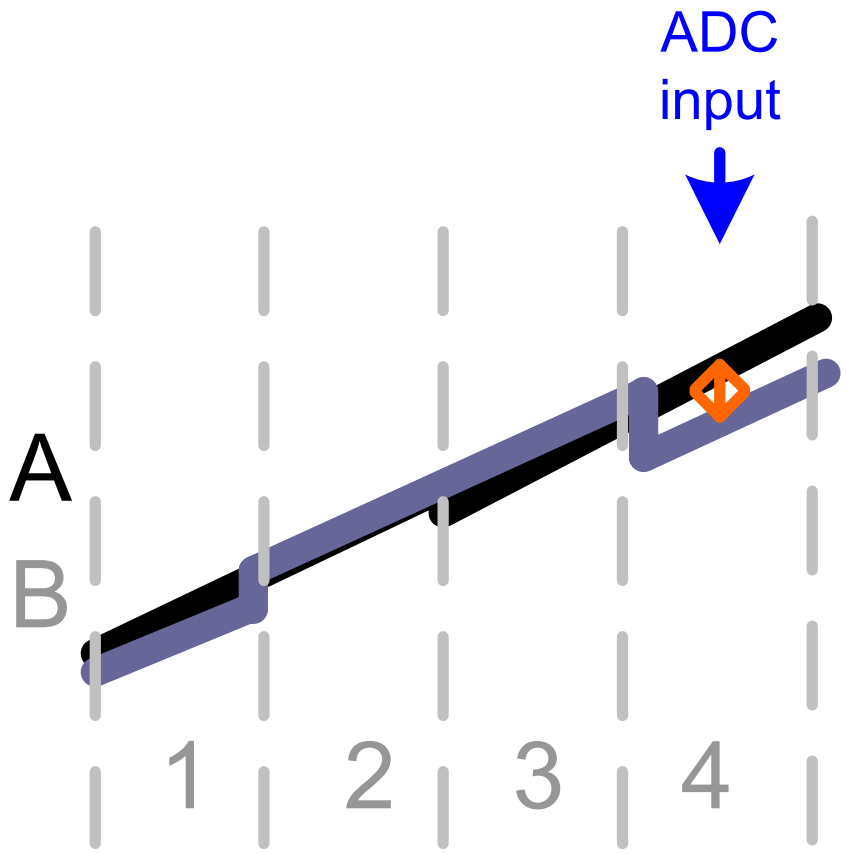
- $\Delta_{A,1} \mathrel{+}= k$, $\Delta_{A,2} \mathrel{+}= k$, $\Delta_{B,1.5} \mathrel{+}= k$, $\Delta_{B,2.5} \mathrel{+}= k$

Calibration example



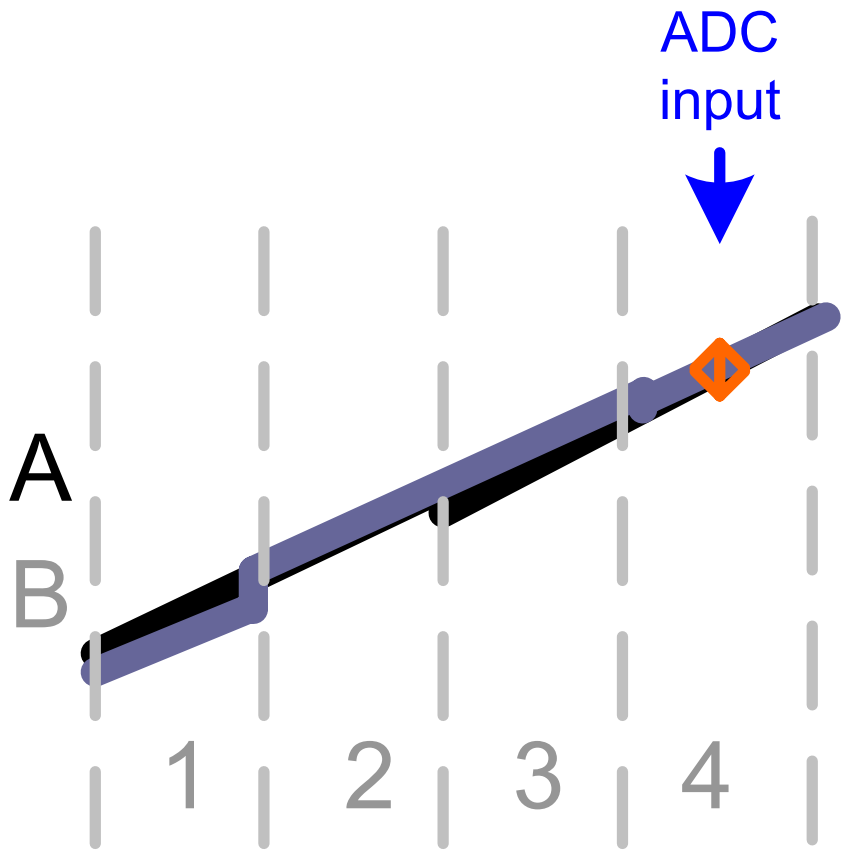
- $\Delta_{A,1}$-= k, $\Delta_{A,2}$-= k, $\Delta_{B,1.5}$-= k, $\Delta_{B,2.5}$-= k

Calibration example



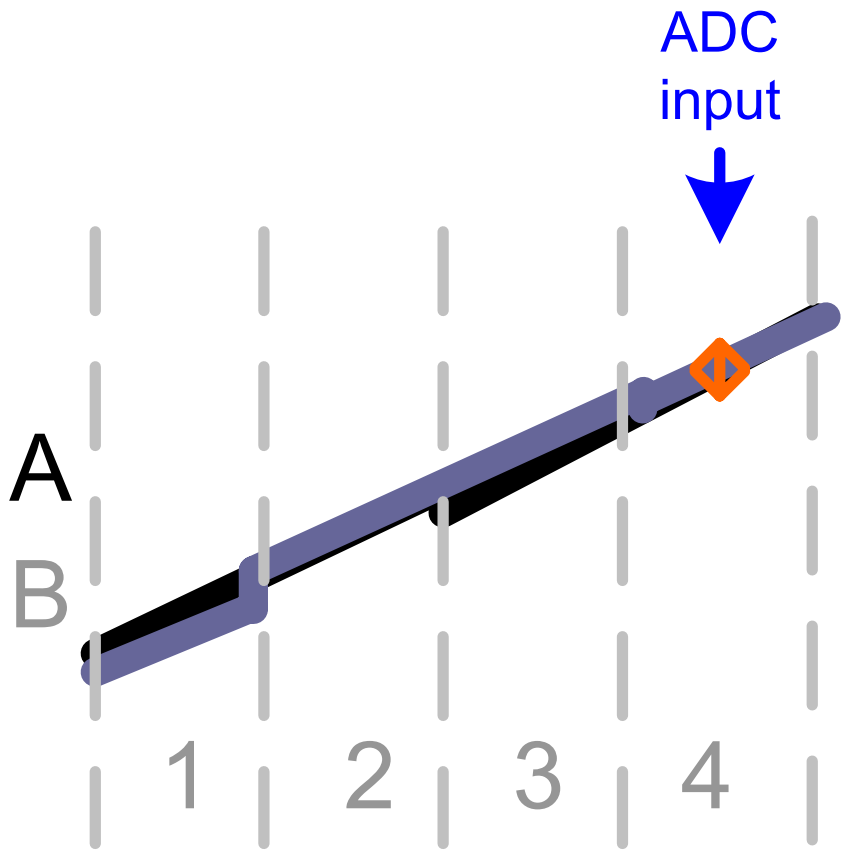
- $\Delta_{\mathbf{B,2.5}}$-= k

Calibration example



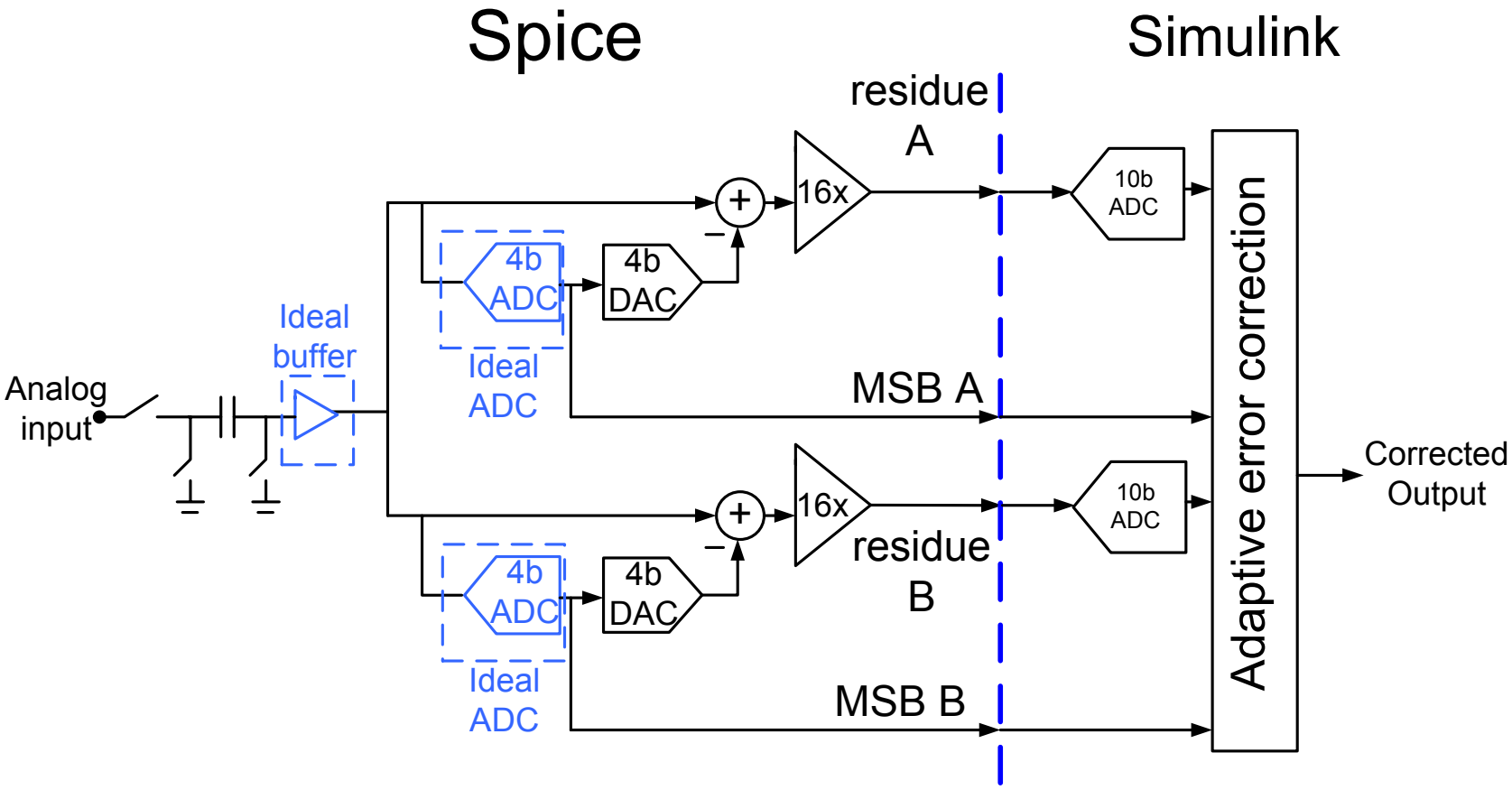
- $\Delta_{\mathbf{B,2.5}} \mathrel{+}= k$

Calibration example



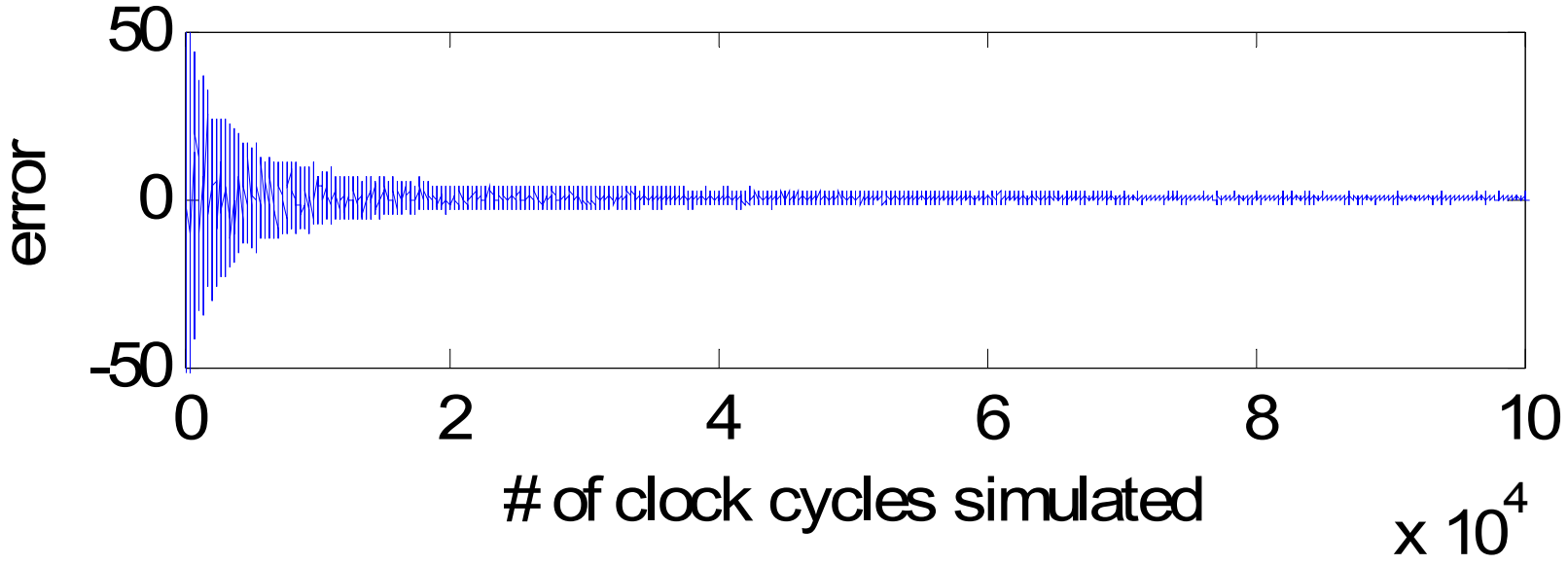
- Random inputs over input range will drive error to zero

Simulations in Spice/Simulink



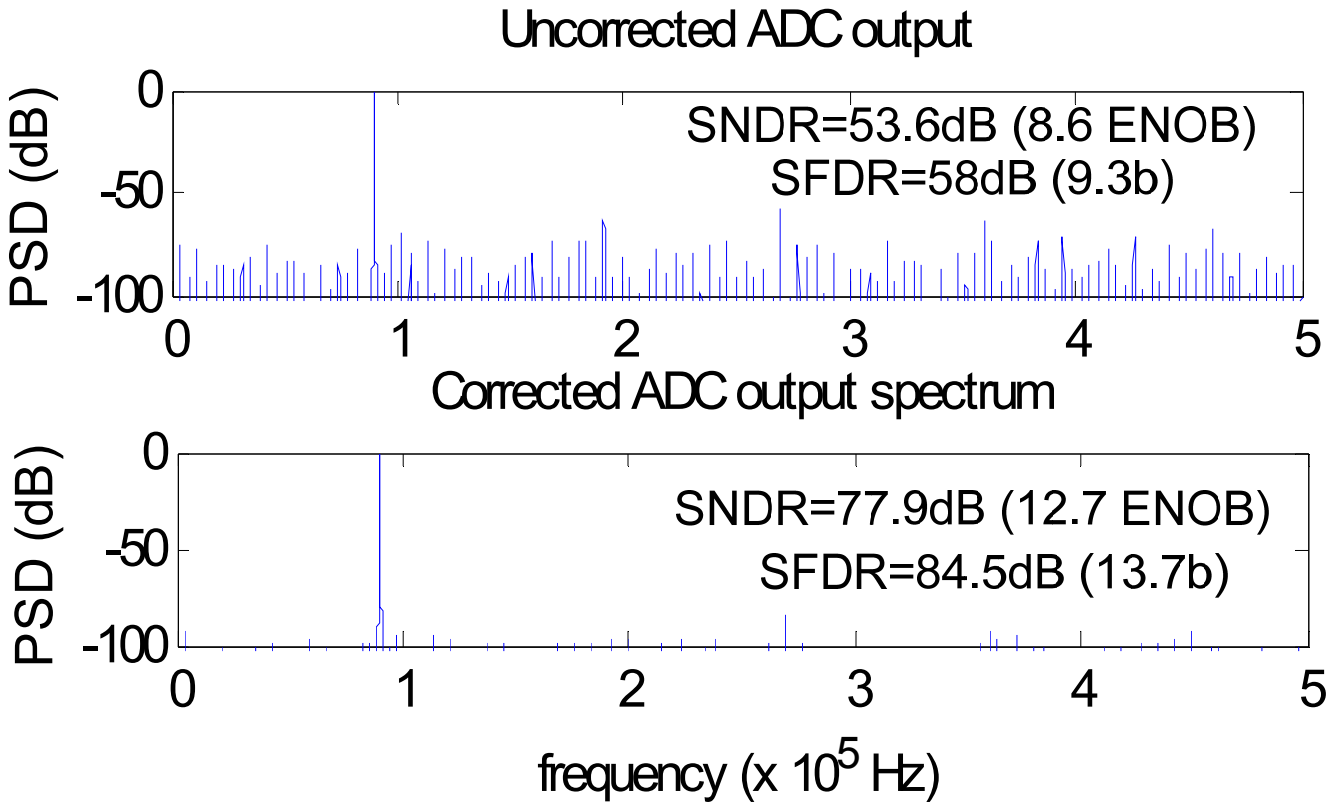
- 12b ADC target, 14 raw bits, 2b extra for calibration
- Front end (MDAC) in Spice, backend in Simulink

Evolution of error signal



- Calibration in less than $10^5 < 2^{17}$ clock cycles, with uniform random input
- statistical approaches need ~10^7 clock cycles for 12b

Output FFTs



- Simulated with opamps of 50dB gain
- Random mismatch in DAC capacitors (peak of ~1%)

Summary

- Overview of Split ADC architecture for pipeline ADCs
- Introduced architecture and algorithm to calibrate DAC errors digitally in the background in short time with Split ADC
- Simulation results in Spice show fast calibration (~10^5 clock cycles) with ~4b improvement in SNDR and SFDR after calibration

Thank you for attending!