ISSCC 2005
Session 15.3

A 50MS/s (35mW) to 1kS/s (15µW) Power Scaleable 10b Pipelined ADC with Minimal Bias Current Variation

Imran Ahmed, David Johns
University of Toronto

Overview

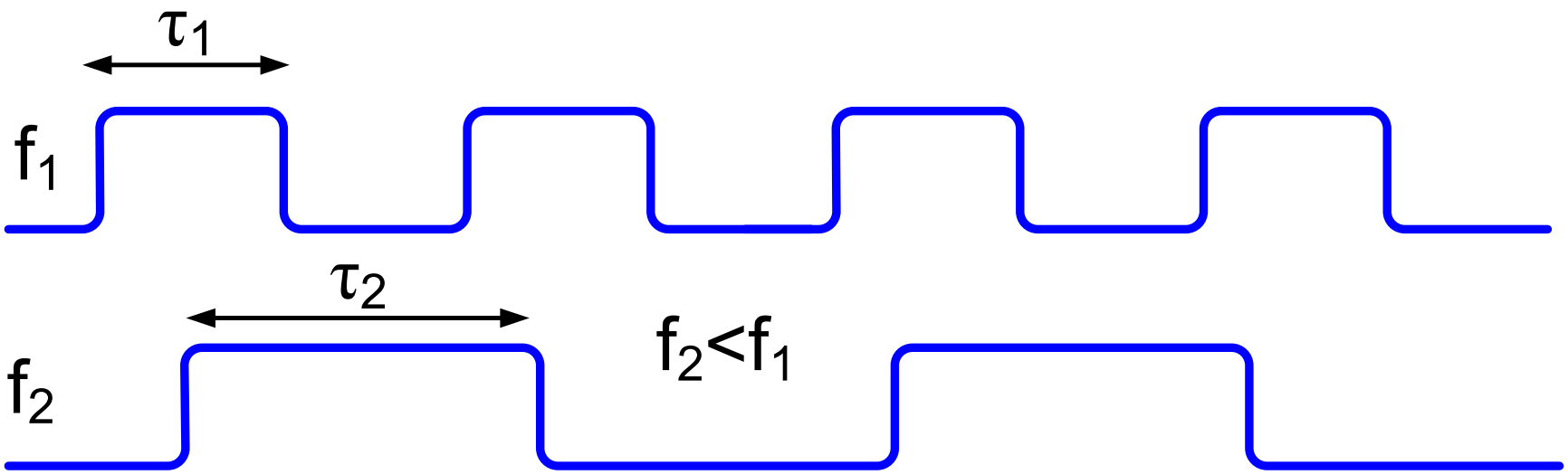
- Motivations
- State of the art
- Approach of this work
  - in 1.8V, 0.18 µm CMOS process
  - Current Modulated Power Scaling (CMPS)
  - New rapid power-on opamp
- Measurement results
- Summary

Motivations

- Applications:
  - Reconfigurable bandwidth, multi-standard, multi-rate
  - Facilitates flexible architecture
- Industrial design
  - Single ADC can target multiple applications
  - Saves development time, thus cost

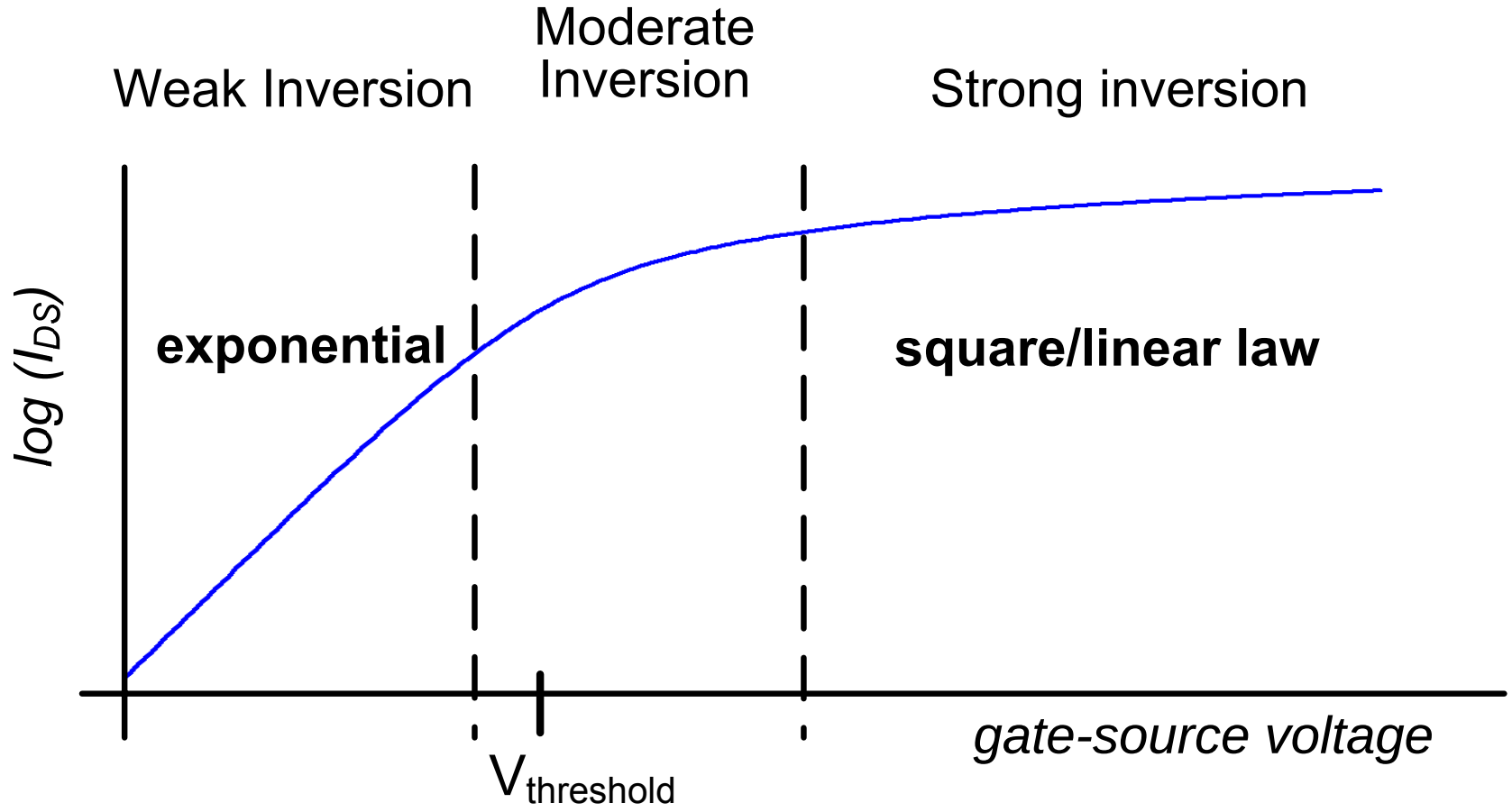
State of the art: Current scaling

$$\tau \propto \frac{1}{I^x} \Longrightarrow$$ as f↓, τ↑ →P=IV↓



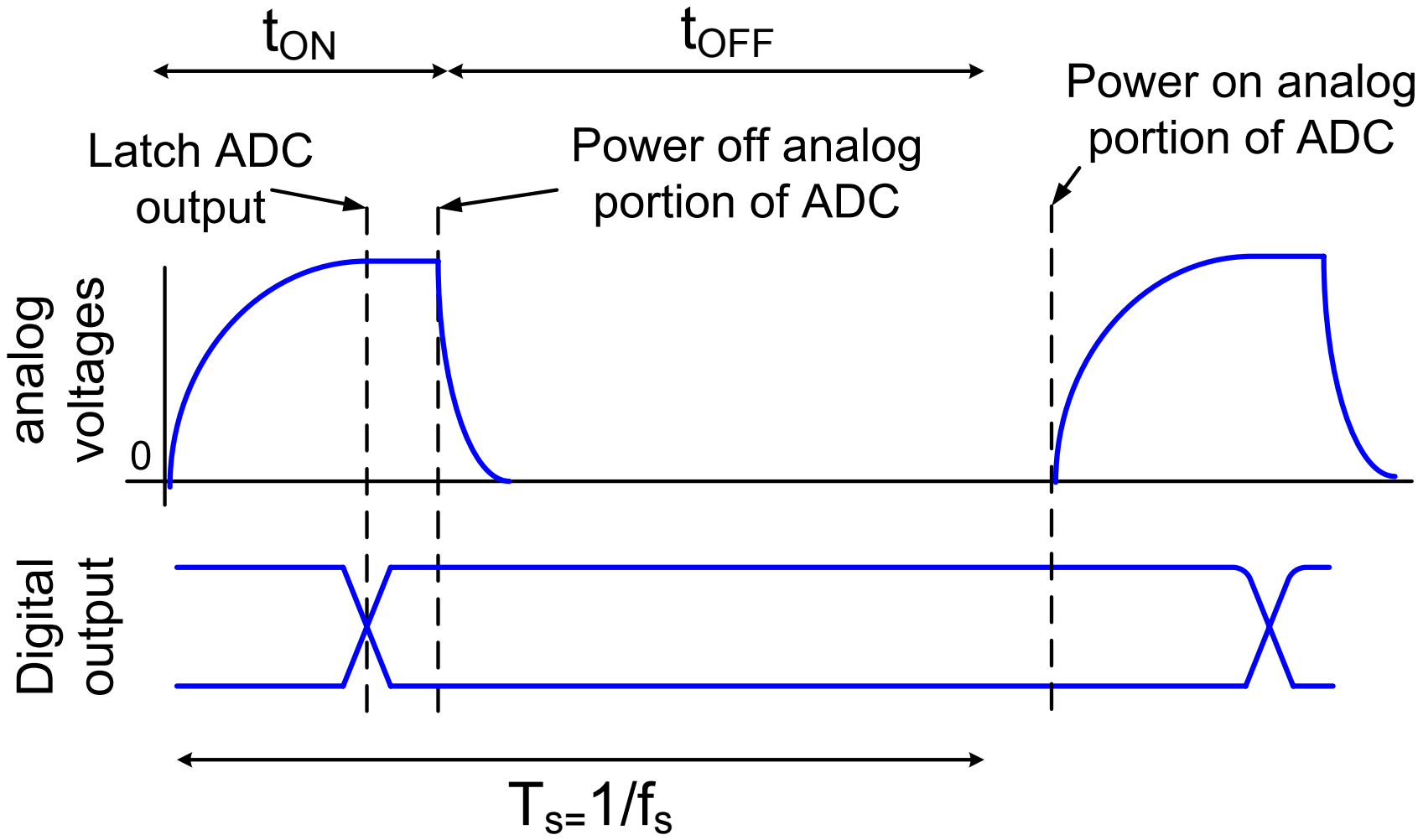
- Analog circuits consume most of the power in ADC
- **Scale bias currents with sampling rate**

Current Scaling (C.S.) implications



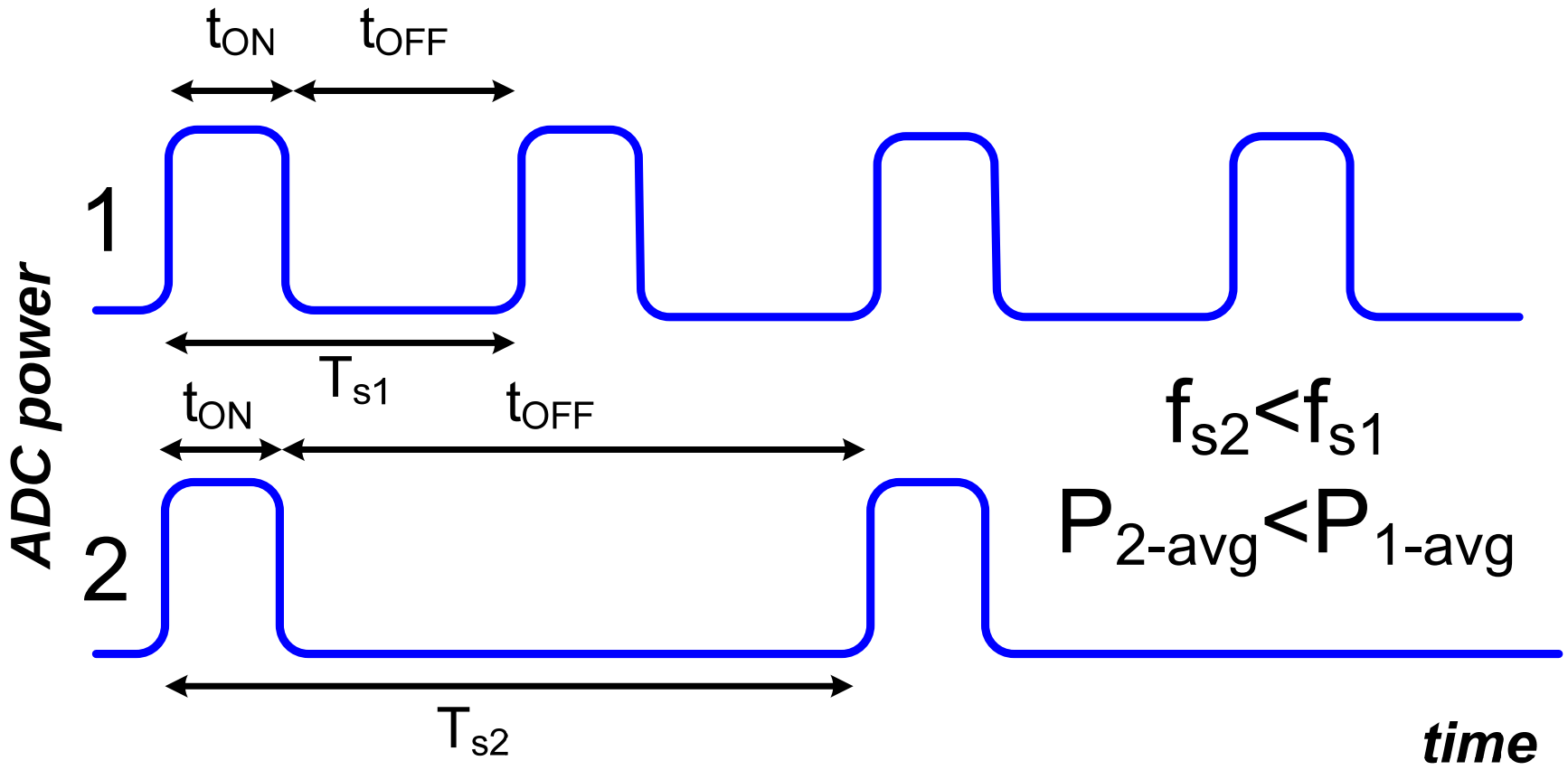
- Greater current mismatch in WI → lower yield
- Multiple bias points → design/verification time ↑

Approach of this work



- Analog power **only** during t_{ON}, digital power during digital output transitions (dynamic power)

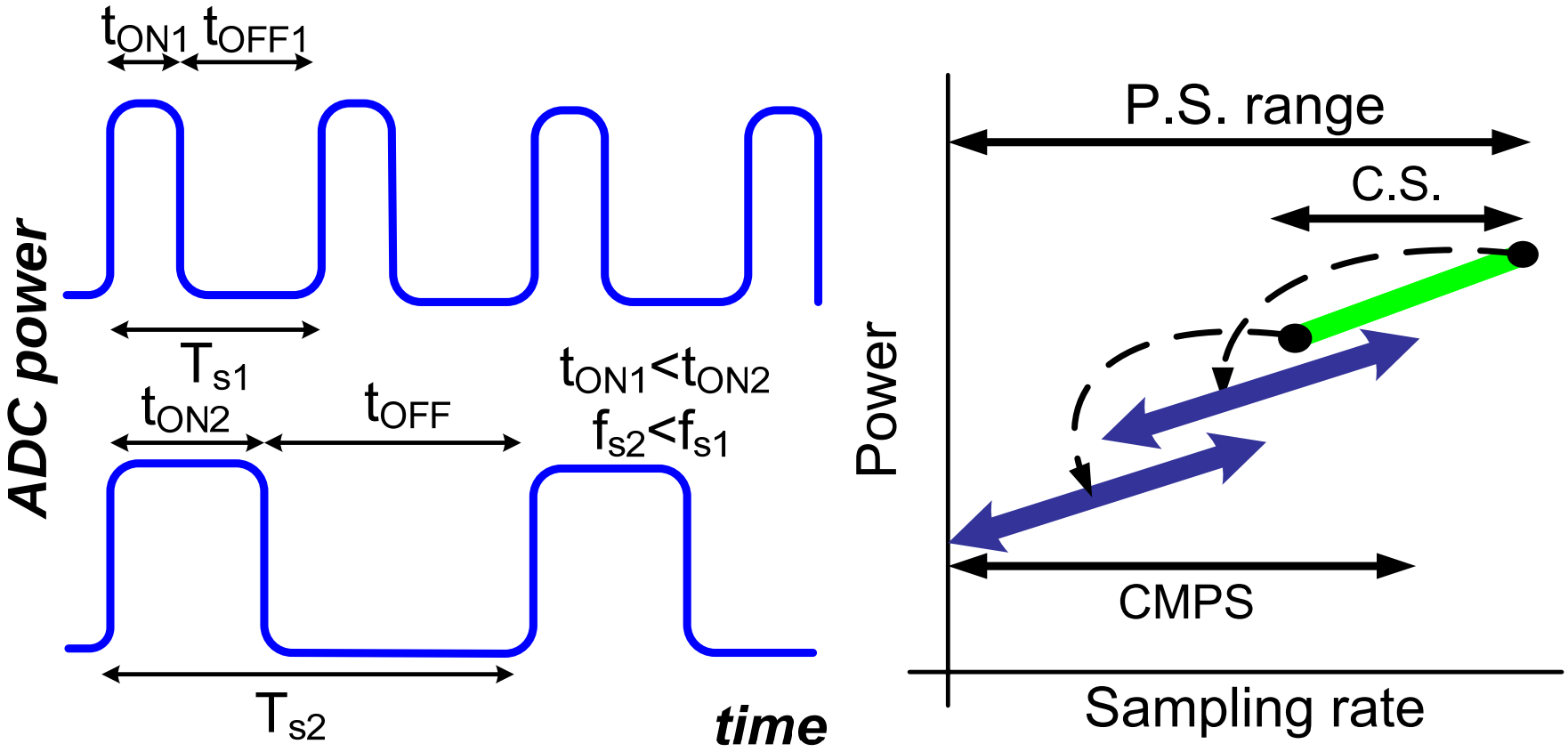
Current Modulated Power Scale (CMPS)



$$P_{avg} = P_{ON}\frac{t_{ON}}{t_{ON}+t_{OFF}} = P_{ON}\frac{t_{ON}}{T_s} = P_{ON}t_{ON}f_s$$

- Constant t_{ON}, variable t_{OFF} to realize different f_s

CMPS with current scaling

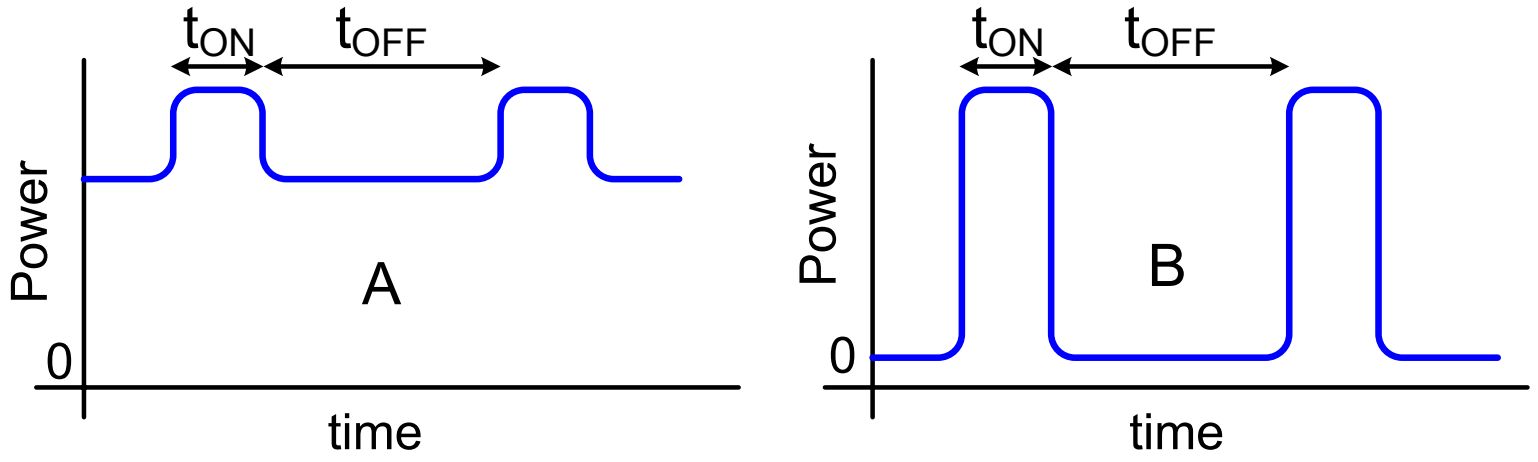


- Variable t_{ON} (f'n of I_B), variable t_{OFF} to realize different f_s

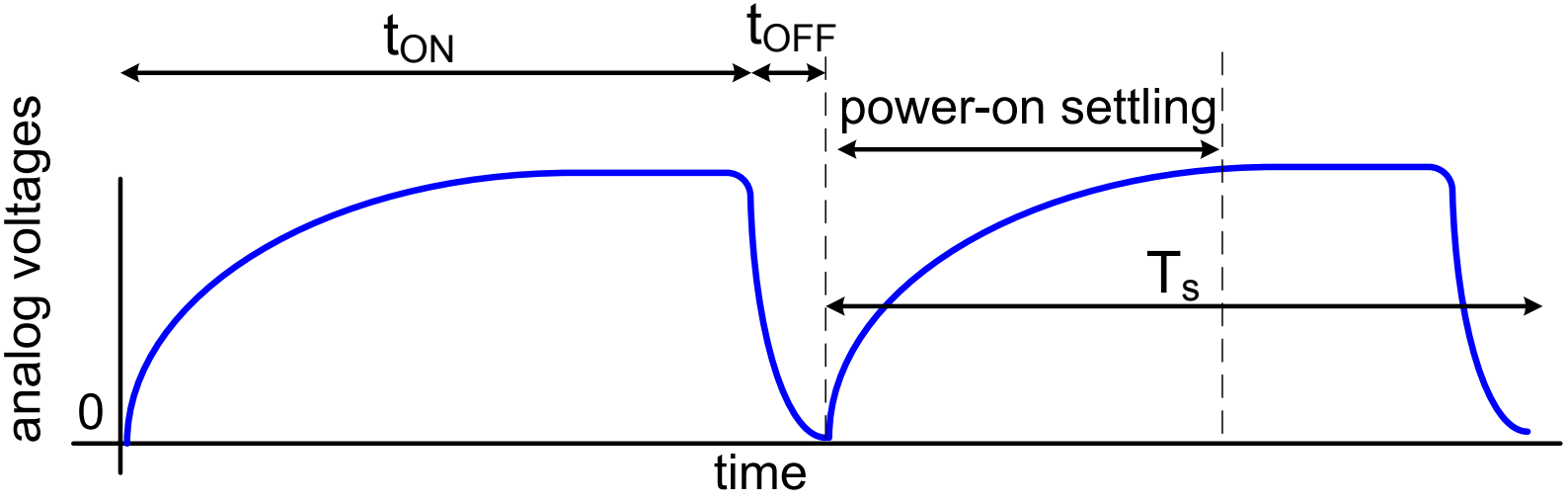
❑ CMPS multiplies CS power scaleable range

Design challenges with CMPS

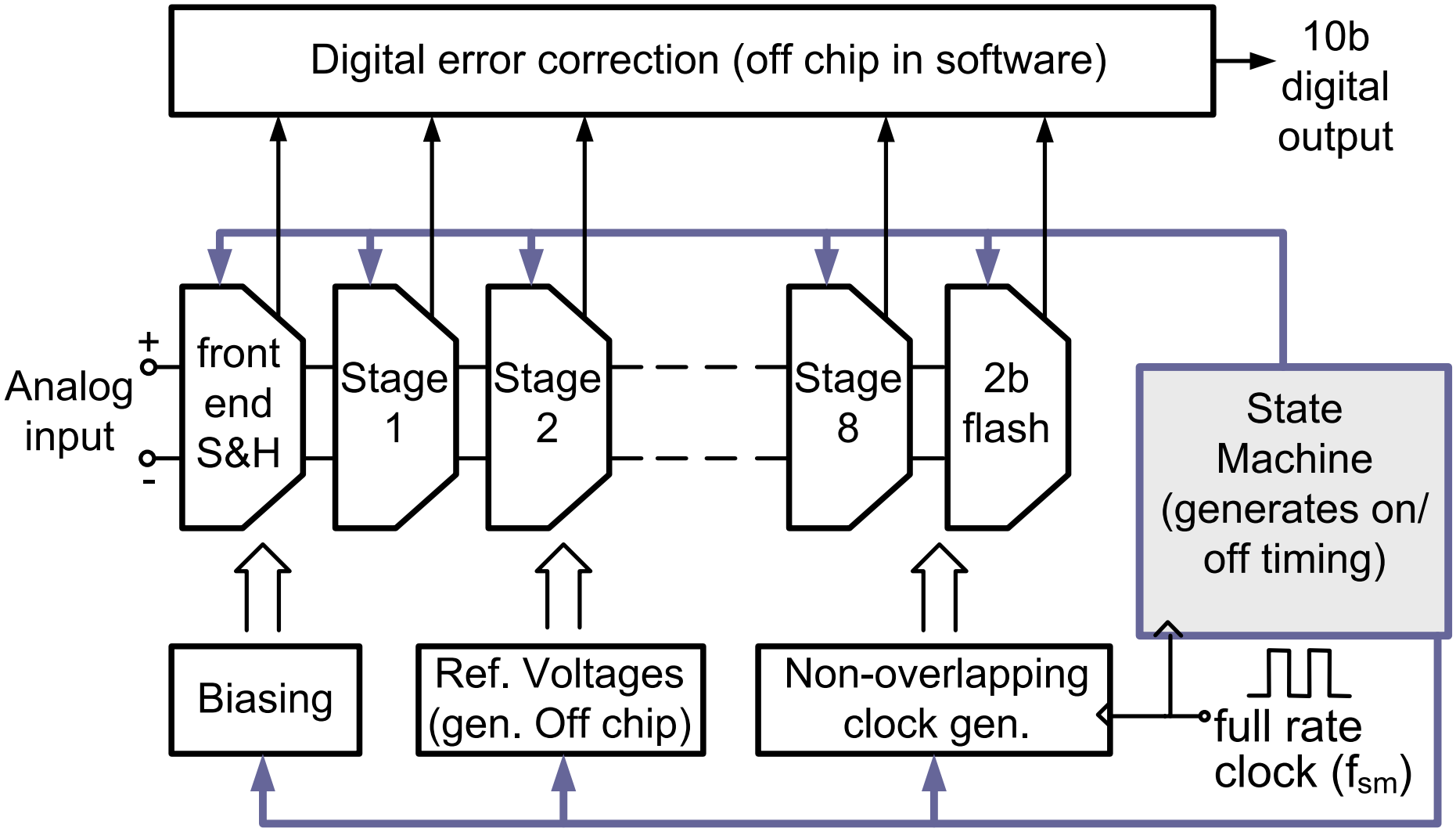
Challenge #1: keep P_{off} low $P_{avg\text{-}A} > P_{avg\text{-}B}$



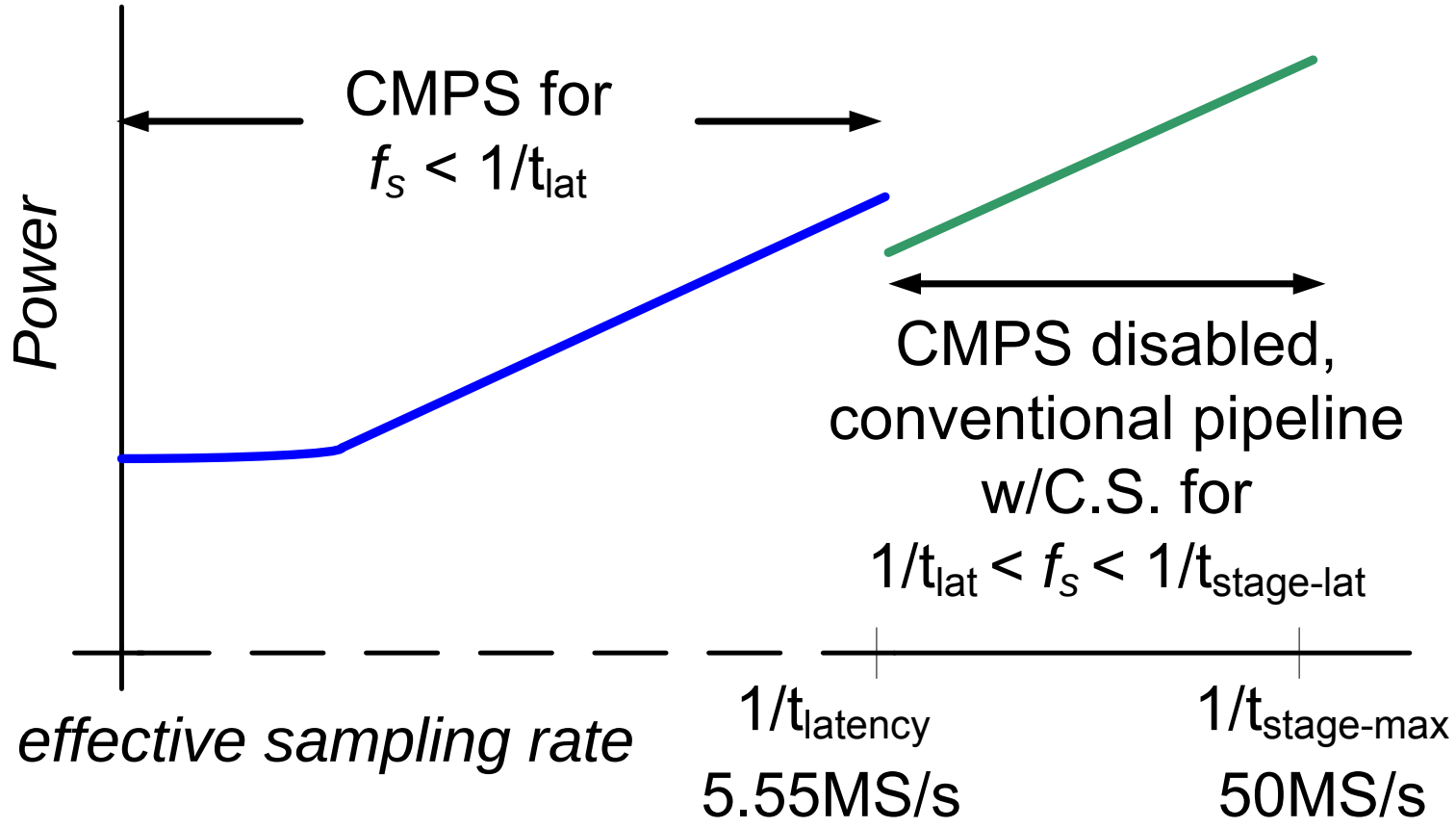
Challenge #2 (key): require rapid power-on to obtain high f_s



10b 1.5b/stage pipeline architecture



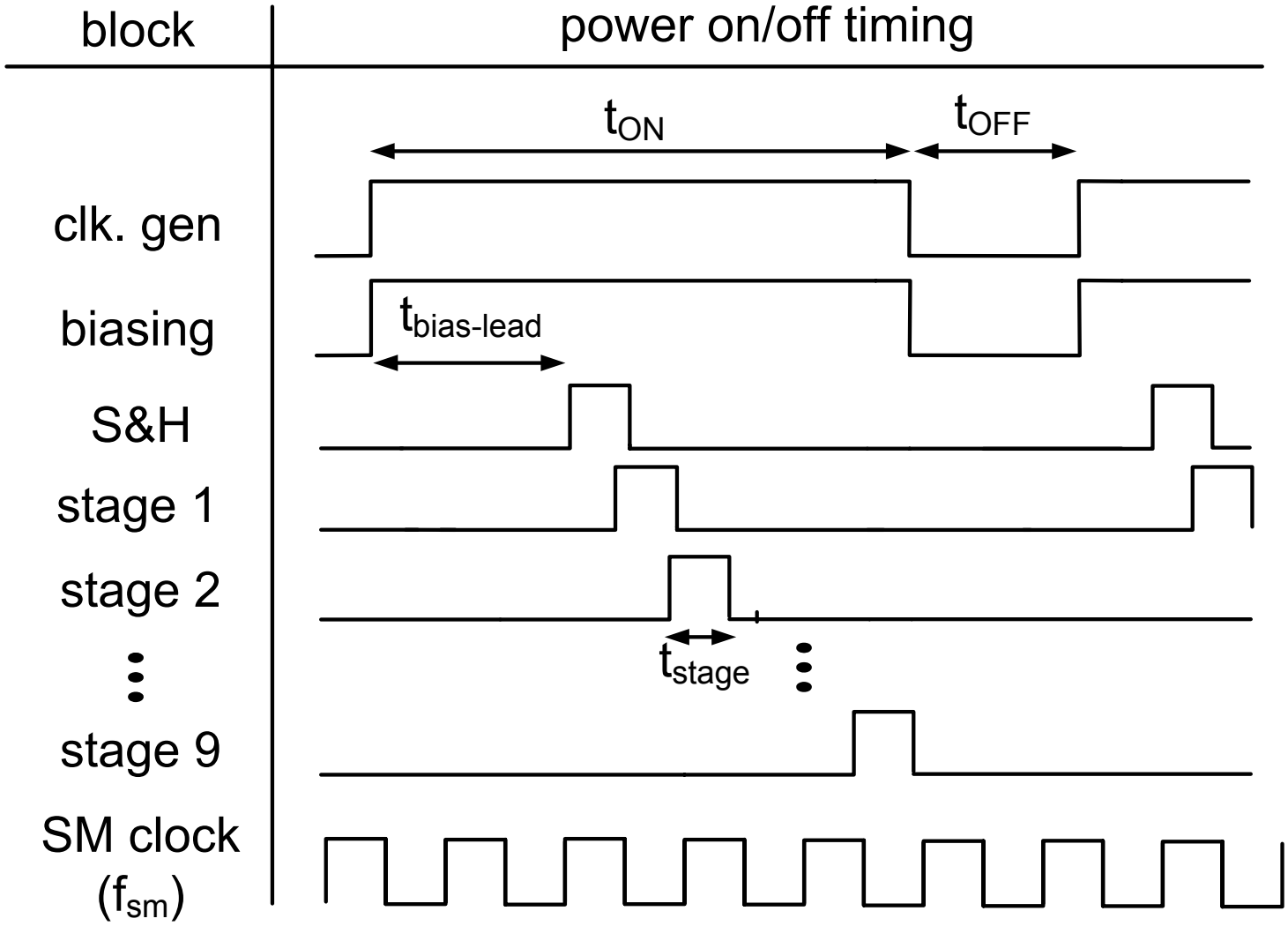
Continuous power scaling



- $t_{ON} = t_{lat}$ (ADC latency) (9 clock cycles)
- Max f_s limited to $1/t_{lat}$ when using CMPS only

❑ Use CMPS + small amount of current scaling

Power timing of pipeline blocks



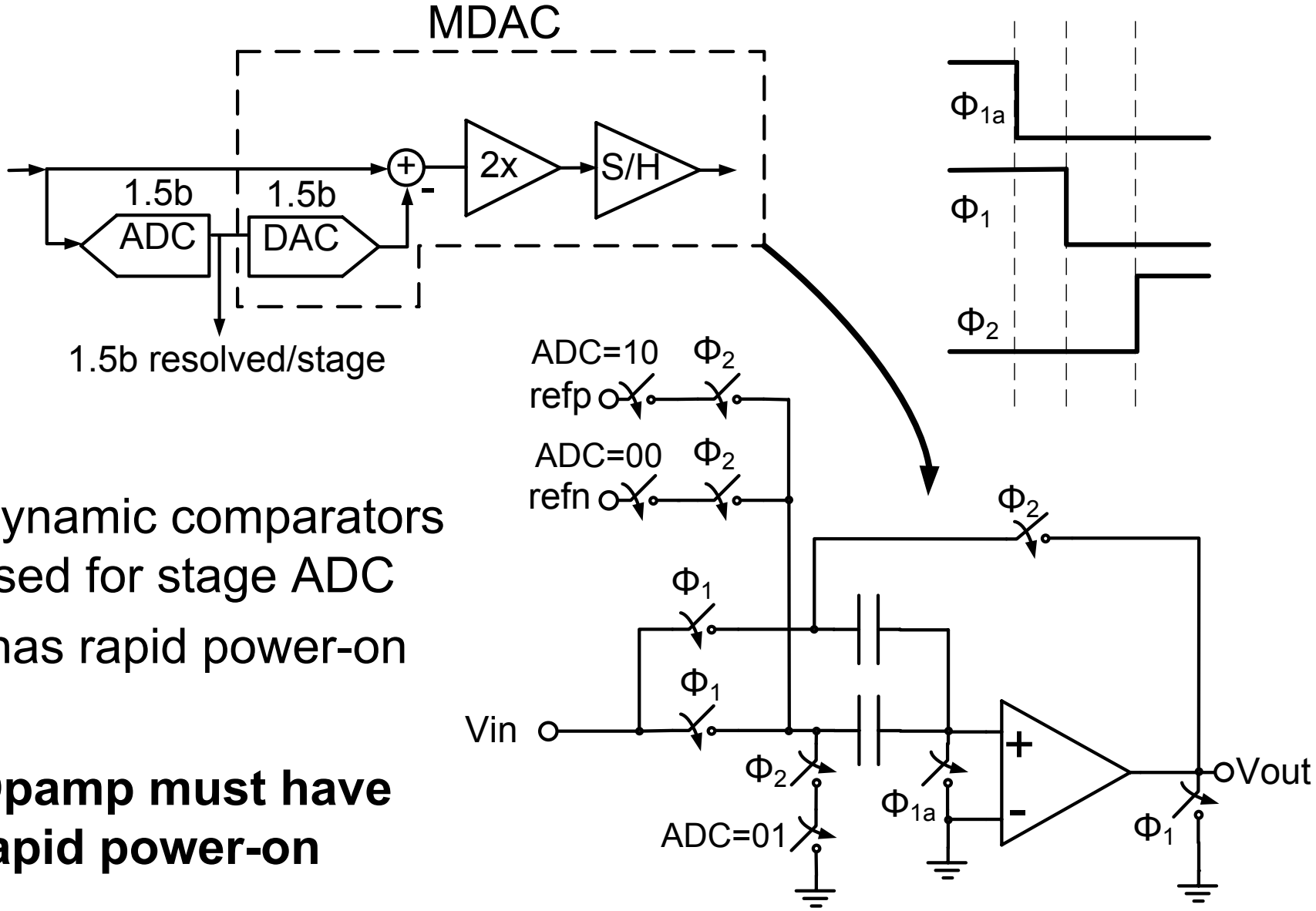
- bias circuits powered on first due to slow power on times

State machine

- always on, dominant power consumer during t_{OFF}
  → limits power scaleable range
- Reducing f_{sm} reduces power during t_{OFF}
  → maximizes power scaleable range

f_{sm}	*State machine Power*
1MHz	9.2μW
5.55MHz	51μW
50MHz	460μW

Stage ADC design

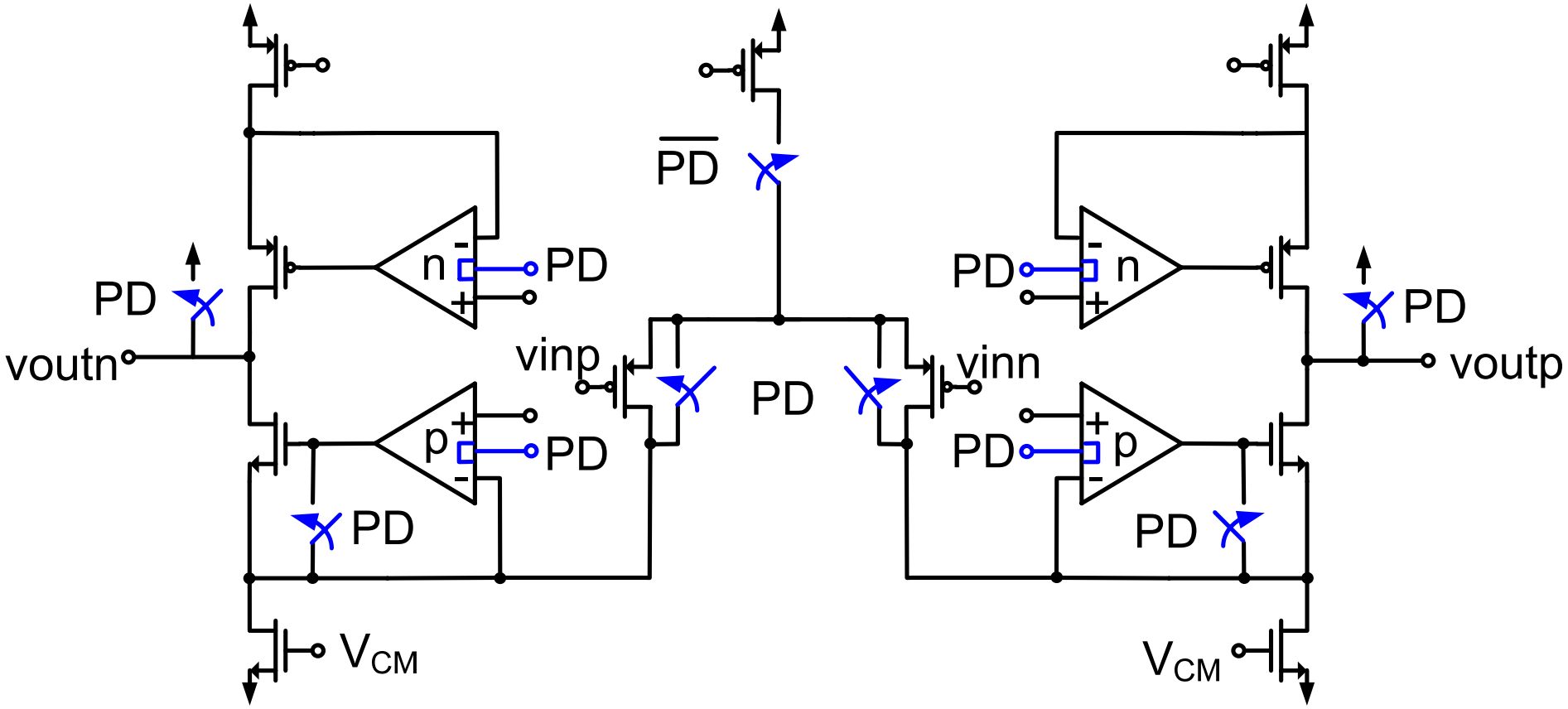


- Dynamic comparators used for stage ADC

→ has rapid power-on

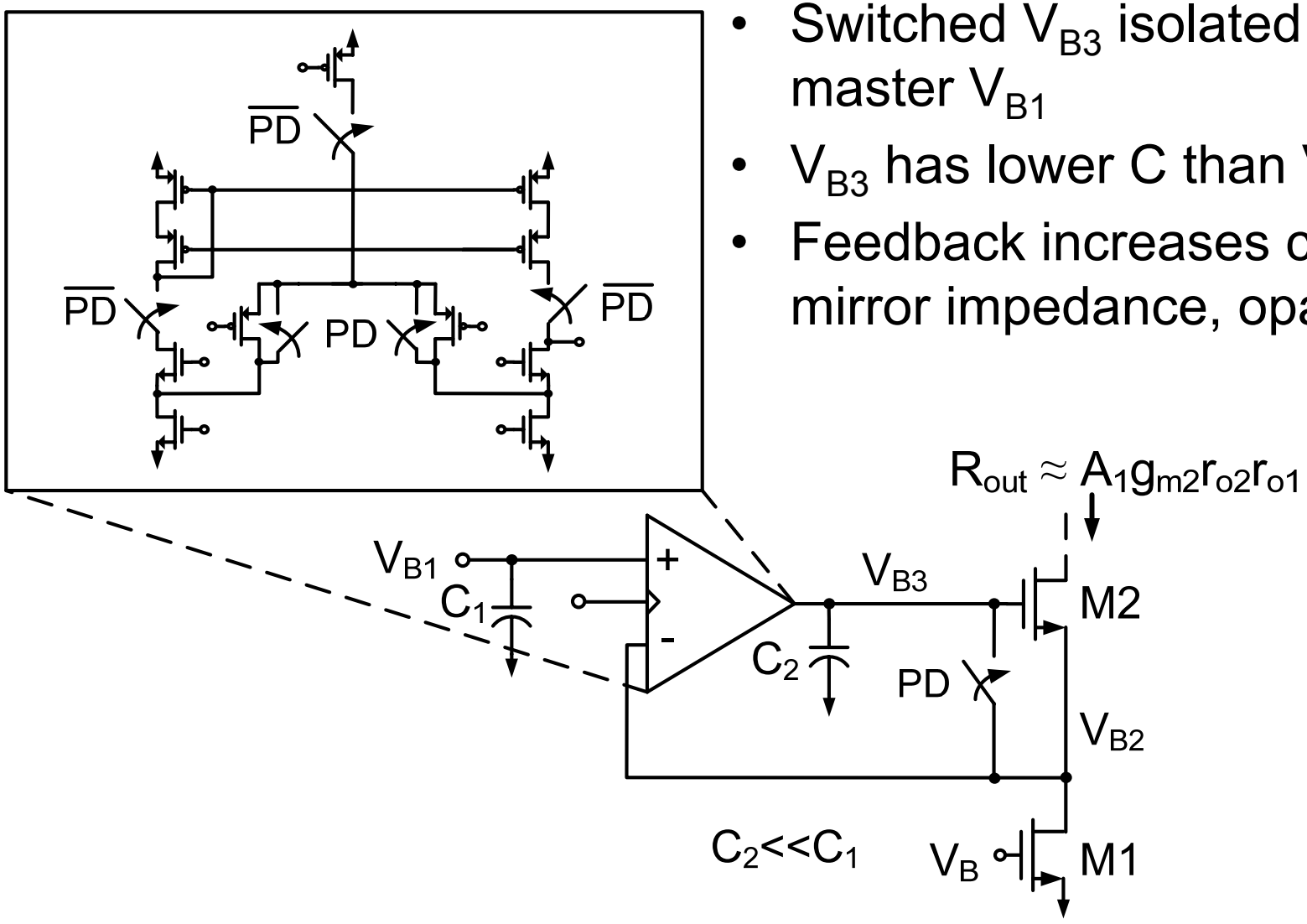
- **Opamp must have rapid power-on**

Rapid power-on opamp



- rapidly powers on during t_{ON}, **<u>completely</u>** powers off for t_{OFF}
- One stage gain → load compensated, simple passive CMFB
- [Waltari, Halonen JSSC Jan. 2001] passive CMFB used

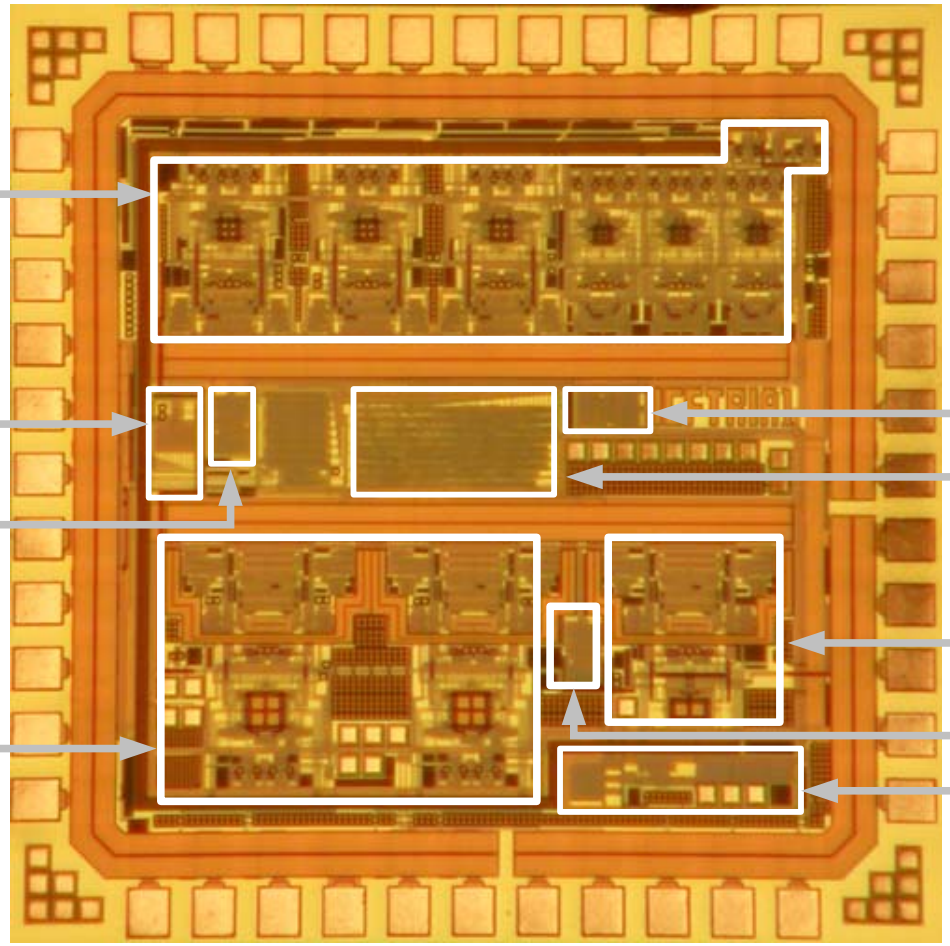
Reduced slew time for rapid power-on



- Switched V_{B3} isolated from master V_{B1}
- V_{B3} has lower C than V_{B1}
- Feedback increases current mirror impedance, opamp gain

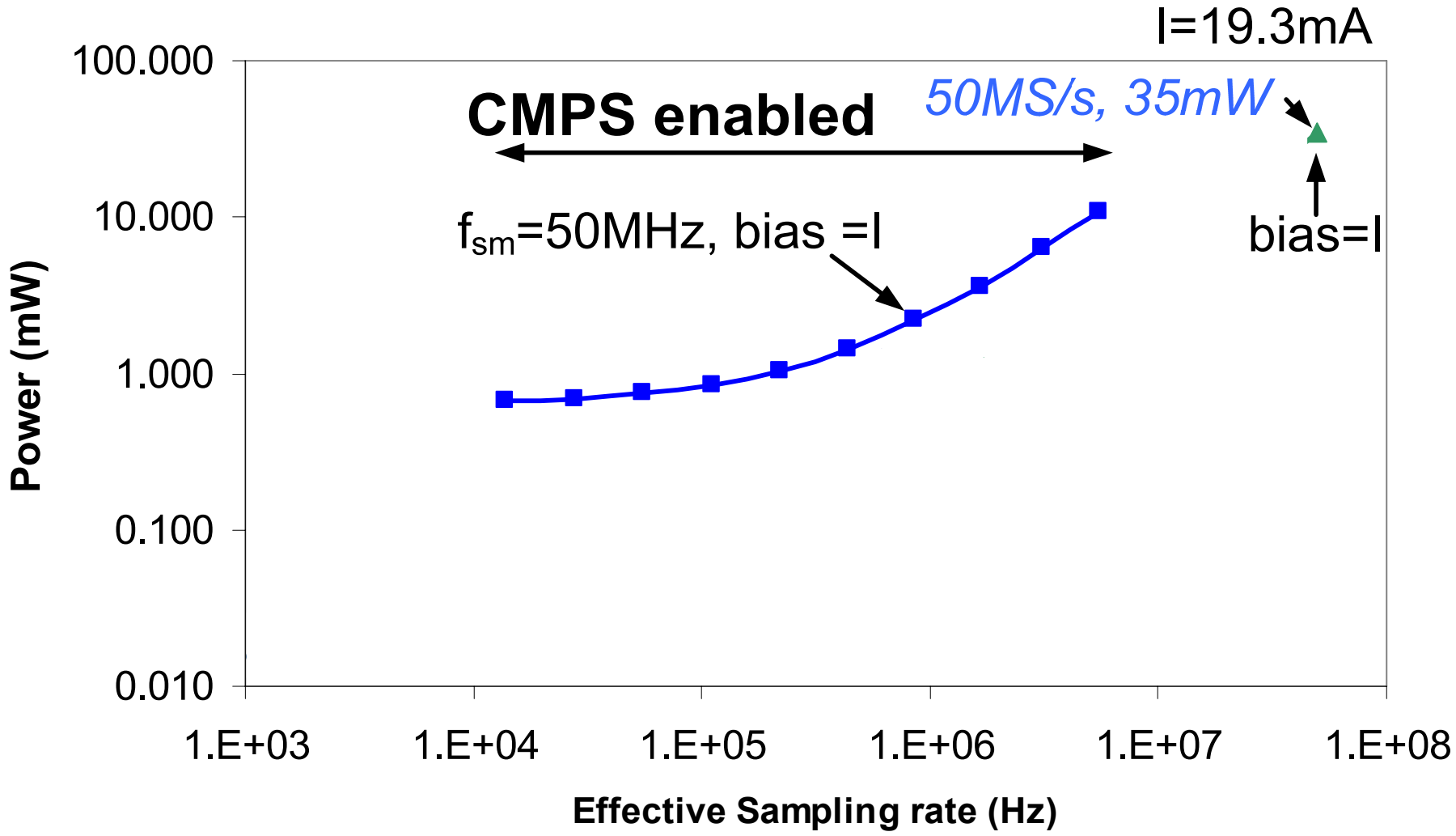
Chip micrograph

1.8V, 0.18µm CMOS

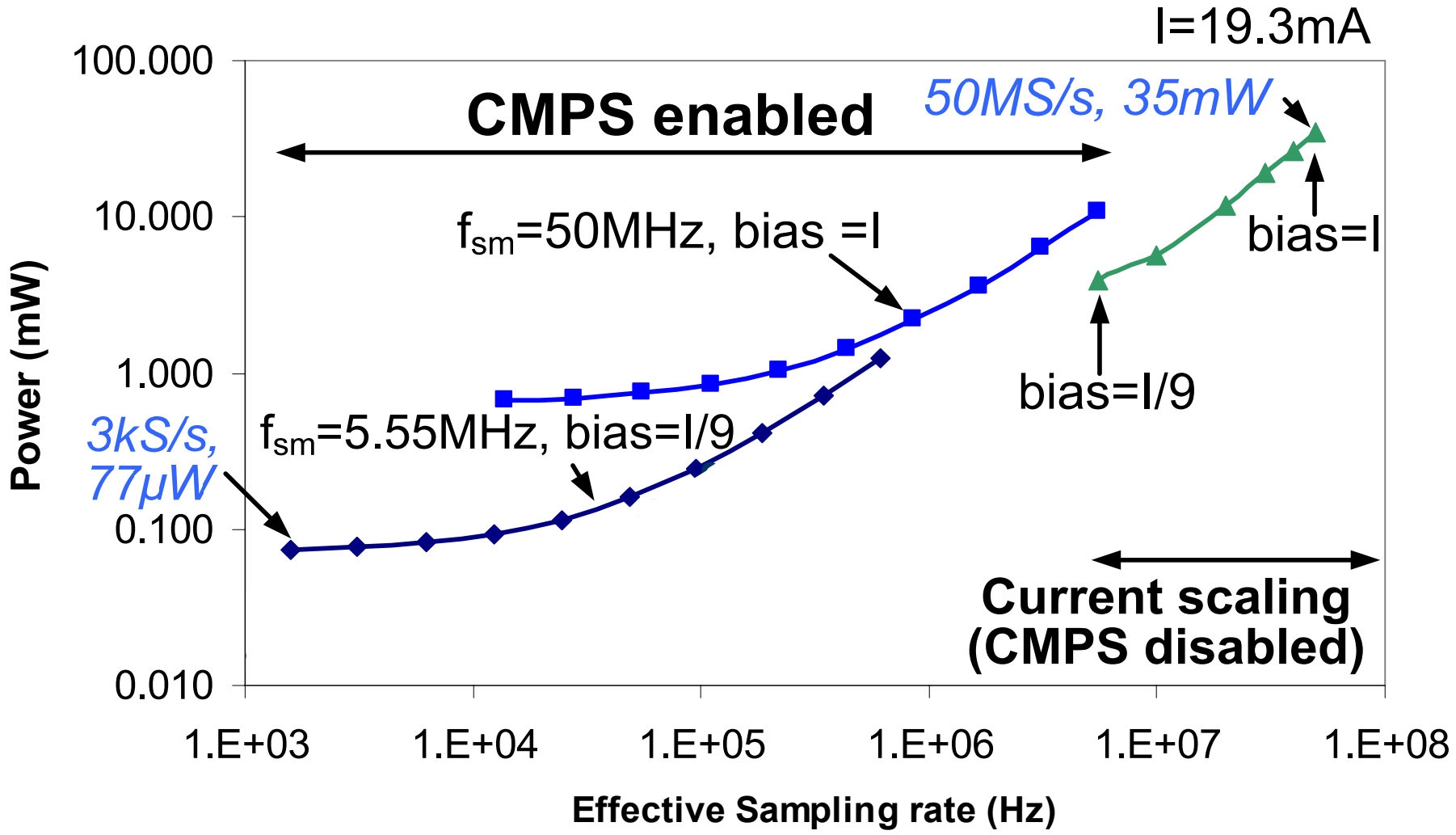


Active area: 1.2mm^2

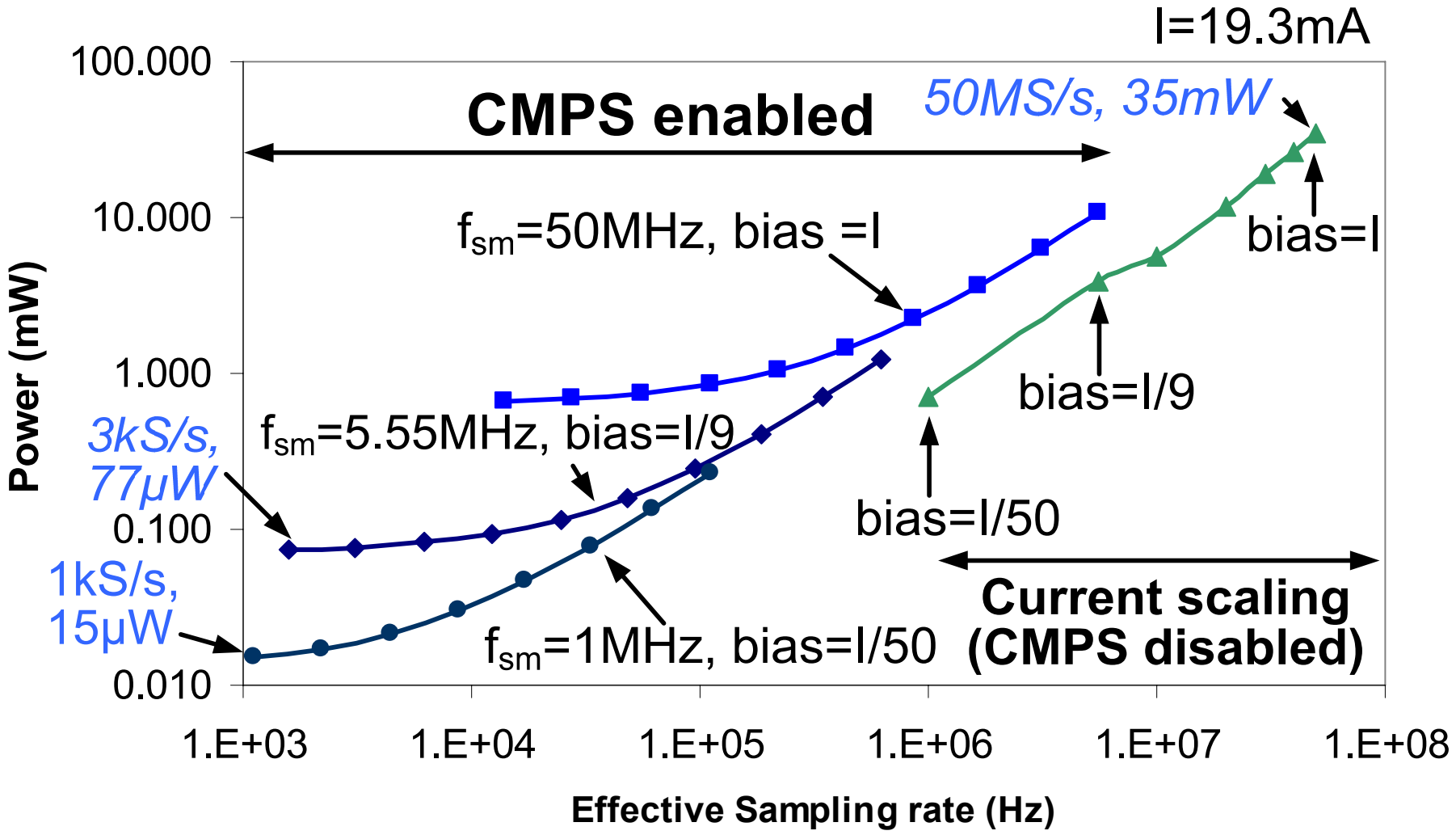
Power dissipation vs. sampling rate



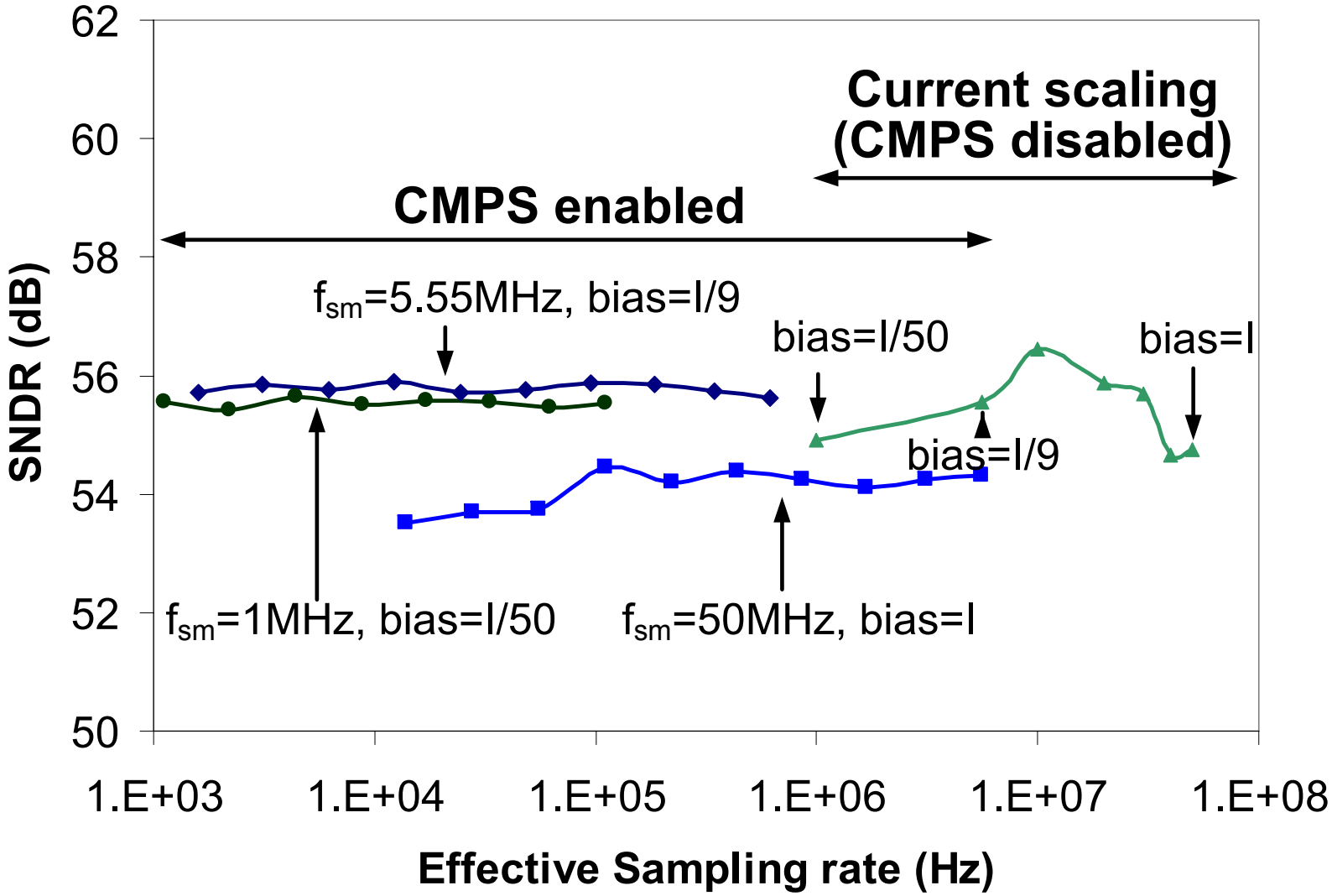
Power dissipation vs. sampling rate



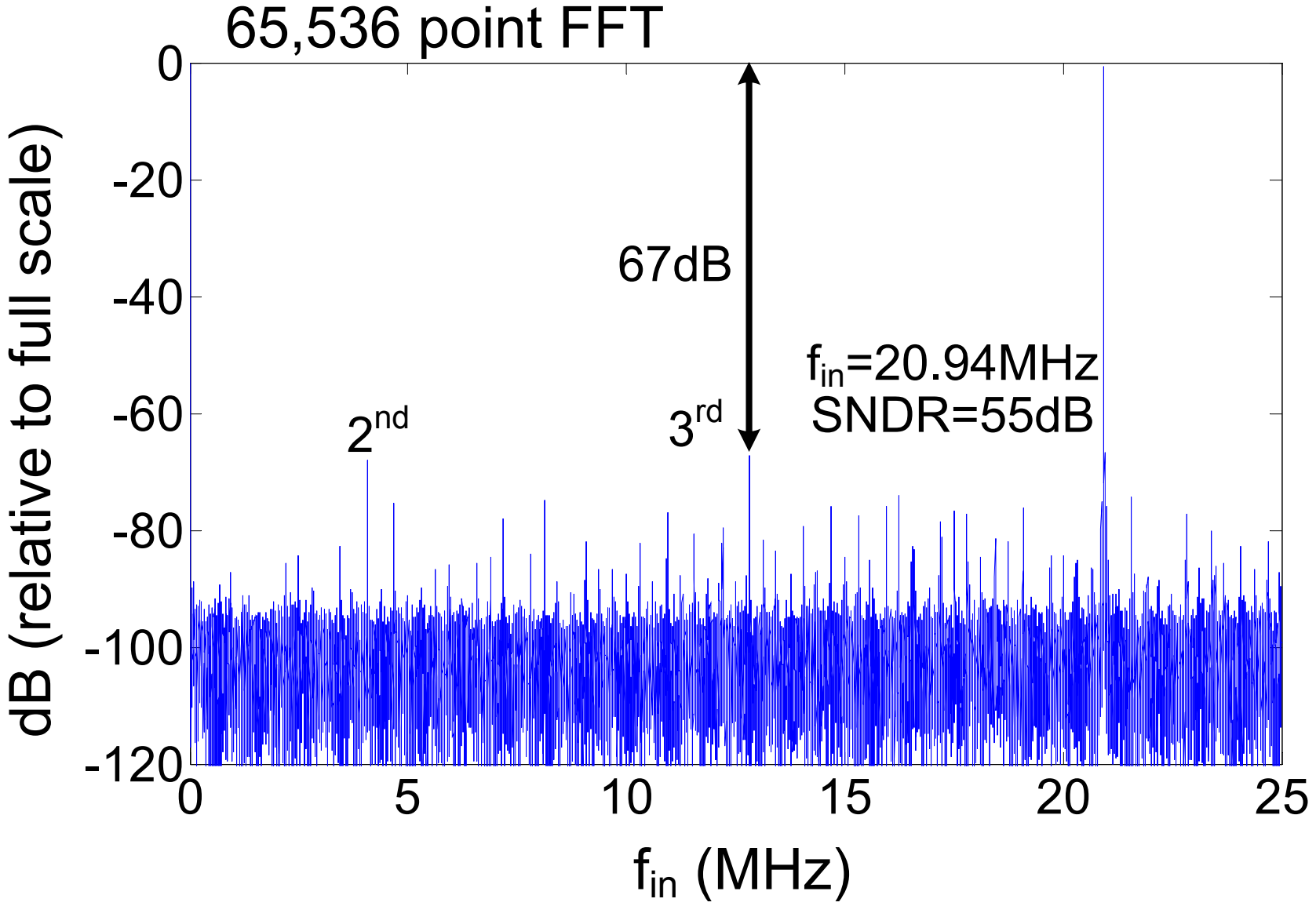
Power dissipation vs. sampling rate



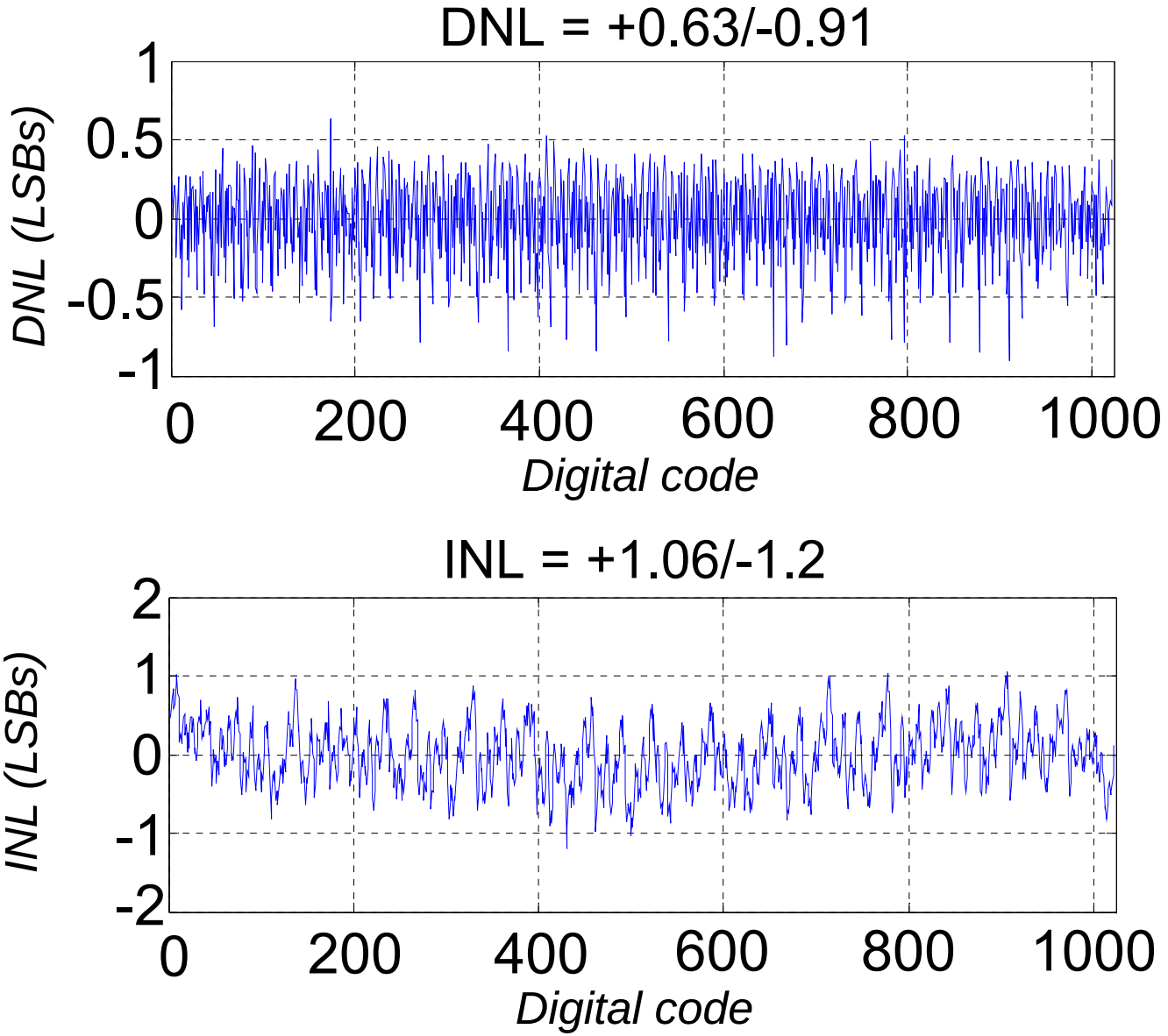
Accuracy vs. sampling rate



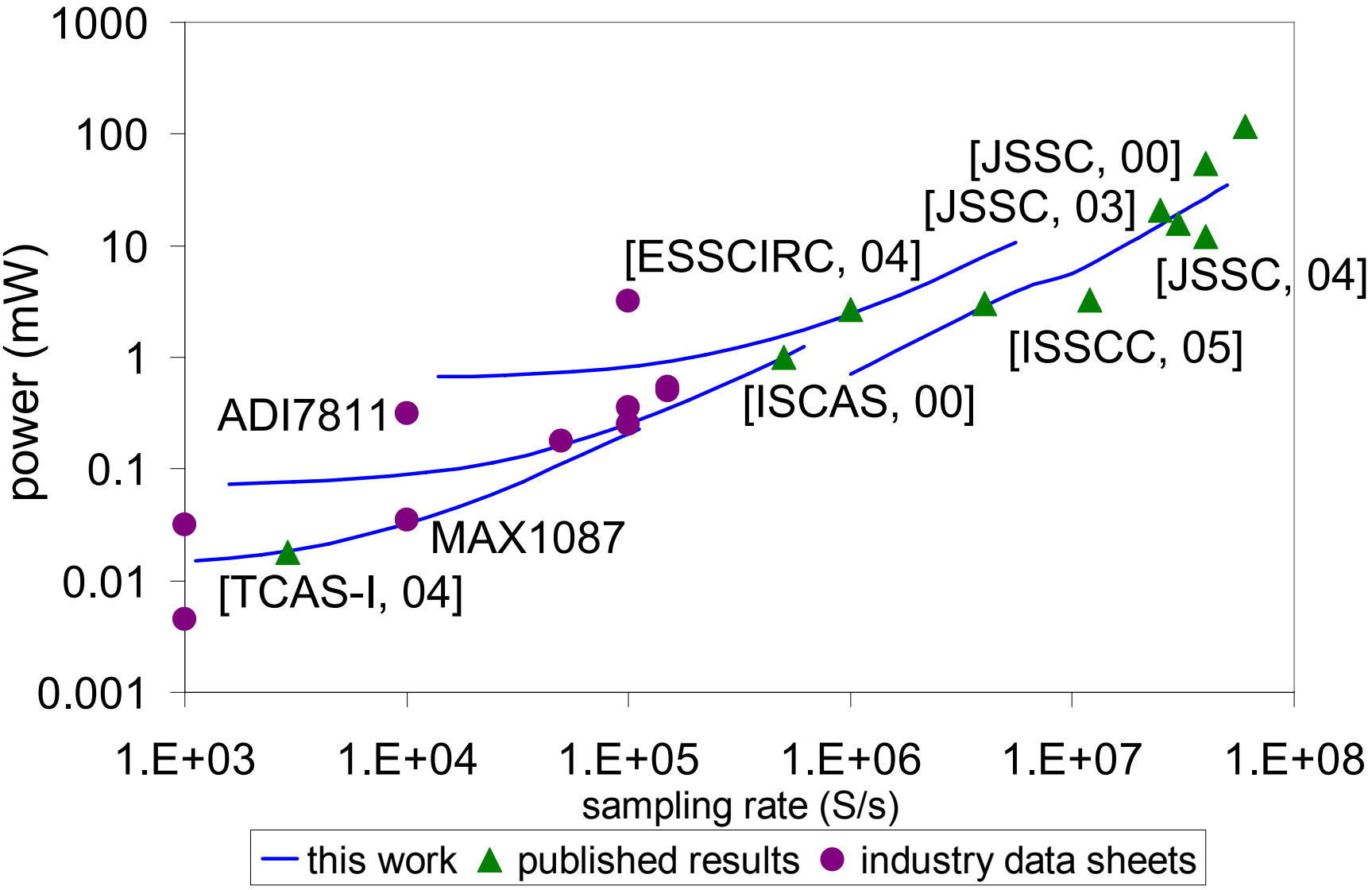
Output spectrum at 50MS/s



DNL and INL at 50MS/s



Comparison with 10b ADCs



Summary

- CMPS used to multiply CS power scale range by 50x to realize very wide power scaleable range
- New rapid power-on opamp enables CMPS at high speeds

Technology	1.8V, 0.18µm CMOS
Resolution	10 bit
Full scale input	1.6V p-p
Area	1.2mm^2
f_s (power) range	1kS/s (15µW) - 50MS/s (35mW)
bias current scaling	1:50
Performance at 50MS/s	
Power	35mW
SNDR (fin=20.94MHz)	55dB (8.8b ENOB)
SFDR (fin=20.94MHz)	67dB
DNL/INL	0.63/-0.91, 1.06/-1.2

Acknowledgements

- Revision help from Professors Ken Martin, K.C. Smith at the *University of Toronto*

- The generous funding from the National Sciences and Engineering Research Council of Canada (NSERC)

- The fabrication services of the Canadian Microelectronics Corporation (CMC)


INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS
ISSCC
UNIVERSITY OF PENNSYLVANIA