A 50MS/s 9.9mW Pipelined ADC with 58dB SNDR in 0.18µm CMOS Using Capacitive Charge-Pumps

Imran Ahmed¹,³, Jan Mulder², David A. Johns¹

¹ University of Toronto, Toronto
² Broadcom Netherlands, Bunnik
³ now with Kapik Integration, Toronto
Overview

• Motivations
• State of the art
• Approach of this work
  – Low power capacitive charge-pump based gain
  – Differential stages without CMFB
• Measurement results
• Summary
Motivations

• **Low power:**
  – Increase battery life in mobile applications
  – Enable cheaper packaging in wired applications

• **Simple topology**

• **Trade analog with digital**
  – Scales better with newer technology
Typical 1.5-bit pipelined ADC stage

- Opamp needed for 2x gain → large power consumer
- Opamp power → gain x bandwidth
State of the art approaches

• Substitute opamp with more power efficient topologies
  – [Murmann et al, ISSCC ‘03]
  – [Sepke et al, ISSCC ‘06]
  – [Hu et al, VLSI ‘08]

• Limitations of prior approaches:
  – Complex topology (e.g. non-linear calibration), or
  – Single-ended/Pseudo-differential, or
  – Linearity below 8-bits
Goal of this work

- Low-power, opamp-free topology that:
  1. A simple topology and digital calibration scheme
  2. Has a differential topology
  3. Can achieve a linearity > 10-bits

- Proof-of-concept Pipelined ADC → 10-bit / 50MS/s
  - Variety of applications from digital communication to medical imaging
2x gain using charge pump

- Capacitive voltage-doubler based approach for gain
during $\Phi_1$

- Input sampled onto two capacitors in first clock phase
- $C1=C2$
• Gain achieved by charge addition
✓ Low power → gain-bandwidth tradeoff decoupled
  x CM error also doubled
Reduced active noise

\[
\frac{4 kT}{3 C_L} \approx \frac{4 kT}{3 C_L}
\]

- Small buffer noise → small capacitors → low power
- Cf. → in SC opamp based circuit, opamp noise directly refers to input
Architectural challenges

1. How to avoid amplifying common-mode errors

2. Impact of parasitic capacitors

3. Topology of unity gain buffer
Impact of common-mode errors

- Small CM offset at input can saturate backend stages
- Need differential pipeline stages

common-mode error multiplied by cumulative gain of stages

n single-ended or pseudo-differential stages
Differential MDAC (+‘ve half)

- Input sampled differentially, no need for CMFB
- $V_{o+}$ common-mode set by common-mode of $V_{DAC+}$
Impact of parasitics on gain

\[ V_{out} = -\frac{C1 + C2}{C2 + C_{p2}} V_{in} + \frac{C1}{C2 + C_{p2}} V_{DAC} \]

- Linear gain error corrected with digital calibration
- Small switches minimize non-linear parasitics
Unity gain buffer – Source Follower

- NMOS S.F. has high $g_m$, low output common-mode
- small input capacitance $\rightarrow \sim C_{gd}$
Complete 1.5-b stage (+’ve half)

- S0 → ensures bottom-plate sampling → good linearity
- S3 → to power-off S.F. for half the clock cycle
Pipelined Topology

- Stage gain ~ 1.75x → need 12 stages for 10-bits
Front-end S/H (half circuit)

- Low-power, simple approach
- Offset of S/H removed by sampler of next stage
Gain error foreground calibration

- assume backend ADC error free
Measurement of gain error

\[ V_{DAC} : \text{ref+} \]
\[ y = \alpha x - \Delta \]
\[ V_{SF-CM} \]
\[ y = \alpha x \]
\[ \text{ref-} \]
\[ y = \alpha x + \Delta \]

- Set \( V_{in} = 0 \), toggle DAC voltage to measure \( \Delta \)
- Recursively calibrate from last stage to first
Chip micrograph

- 1.8V, 0.18µm CMOS process
- 1.4 mm² includes test circuitry, decoupling caps.
32,768 pt FFT ($f_{\text{in}}=2.4 \ \text{MHz}$)

- Even order distortion strongly suppressed

SNDR = 58.2dB
ENOB = 9.4 bits

SFDR = 66dB

$f_s=50\text{MS/s}$
32,768 pt FFT ($f_{in} = 20.7$ MHz)

- SNDR = 56.9 dB
- ENOB = 9.2 bits
- $f_s = 50$ MS/s
- SFDR = 65 dB

> 9-bit ENOB for Nyquist bandwidth
\[ f_s = 50 \text{MS/s}, \text{ SNDR/SFDR } \text{ vs. } f_{\text{in}} \]

- **Power:** 3.9mW (active) + 6mW (clocking) = 9.9mW
- **Ref. voltages (not included)** → 0.34mA
INL (before calibration)

- Peak INL = +15.7/-17.9 LSB (LSB @ 10-b level)
INL (after calibration)

- Peak INL = [+0.7/-0.8] LSB
• Peak DNL = +1.6/-1 LSB
• Peak DNL = \(+0.35/-0.35\) LSB
Calibration robustness

• Calibration coefficients fixed, ADC output measured while varying:
  – Bias currents by +/-10%
  – Time interval as long as 1 week

• ENOB varied less than 0.05-bit

• Gain error not a strong function of bias currents, drift → may not require frequent calibration

• use background calibration to track temperature
Comparison to other 10-b ADCs

- FOM of this work = 0.3pJ/step
Summary

- Low-power gain with capacitive charge-pumps
  - Differential
  - linearity > 10bits
  - Low complexity architecture

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